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MS-7362

Version : 1.0

CPU :

Intel Conroe Family and Kentsfield Family Processor
Intel Pentium D Processor 900 and 800 Sequence
Intel Pentium 4 Processor 600 Sequence

System Chipset :

Intel G965 - GMCH (North Bridge)
Intel ICH8 (South Bridge)

On Board Chipset :

Clock Gen. -- ICS9LPRS514
Azalia Codec - ALC883 / ALC888
LAN -- RealTek RTL8111B / RTL8101E
VRM 11 - Intersil 6312 / 6322
ACPI Controller -- MS7 / MS11
IEEE 1394 -- VIA VT6308P
PATA -- Marvell 88SE6111
TPM 1.2 -- Infineon SLB9635TT1.2
Super I/O -- Winbond W83627DHG
SPI Flash 8Mb

Main Memory :

2 Channel DDR II * 4 (Max 8GB)

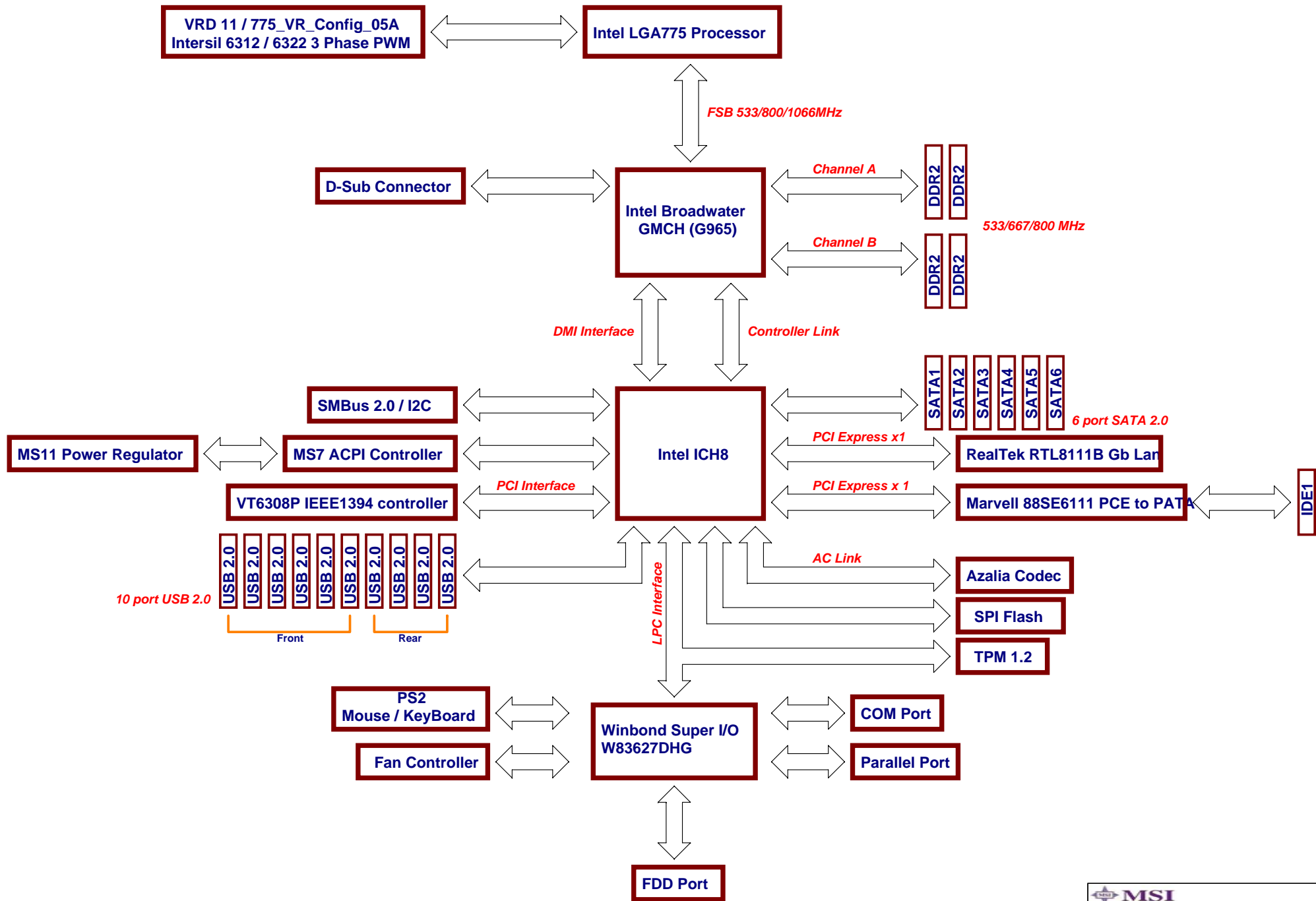
Expansion Slot :

PCI Express x16 Slot * 1
PCI Express x1 Slot * 1
PCI Slot * 2

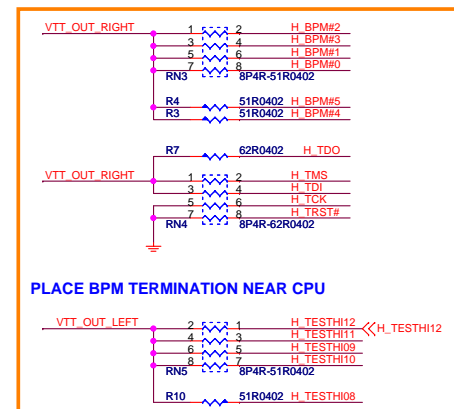
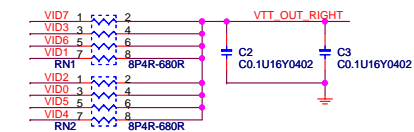
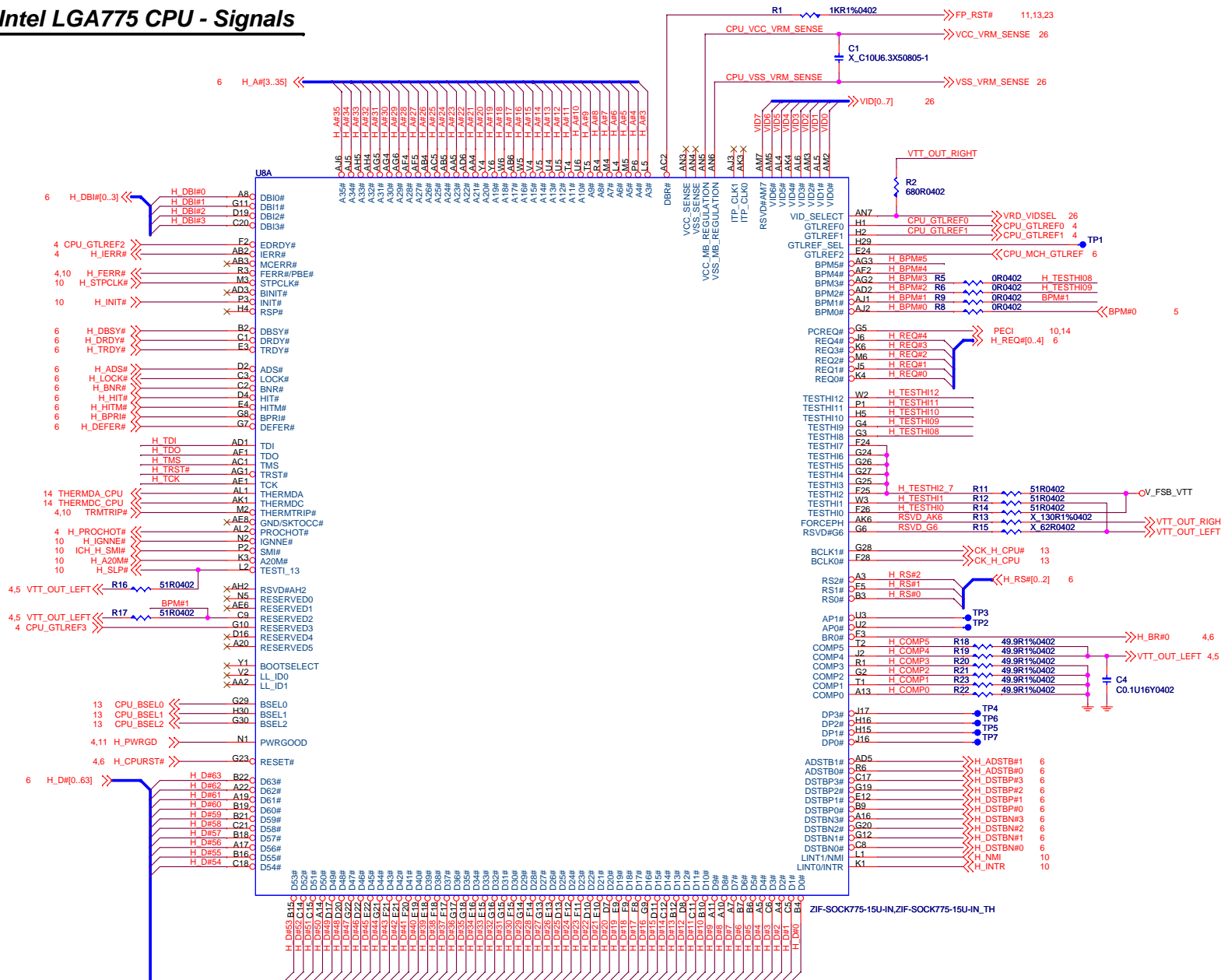


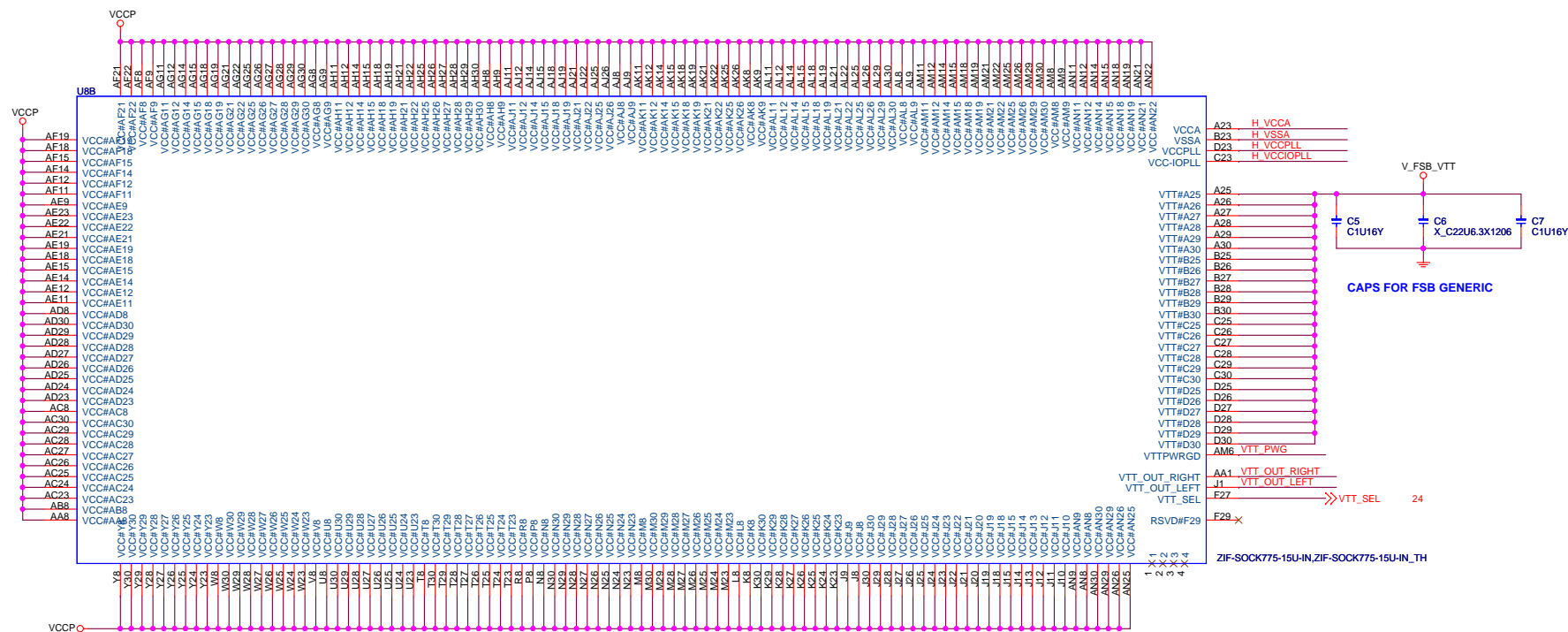
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7362-01S	Cfg-STD	G965 + ICH8 + RTL8111B + ALC888 + VT6308P + 88SE6111 + W83627 DHG	STD
7362-02S	Cfg-L	G965 + ICH8 + RTL8111B + ALC888 + VT6308P + 88SE6111 + W83627 DHG	L

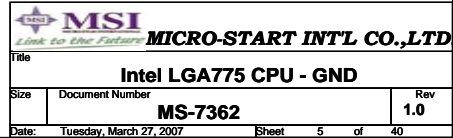
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Title Cover Sheet		
Size	Document Number	Rev
	MS-7362	1.0
Date: Tuesday, March 27, 2007	Sheet 1 of 40	

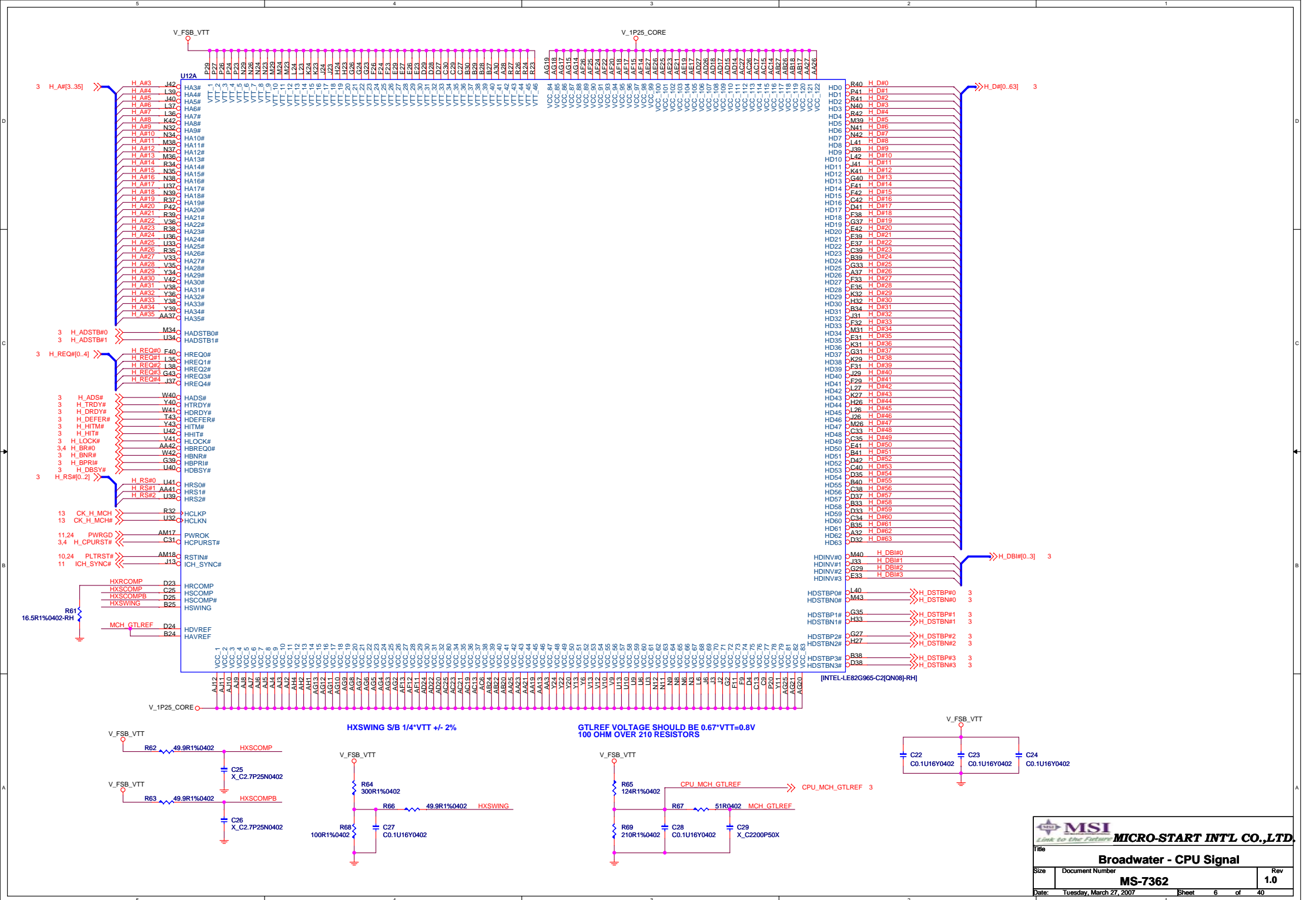


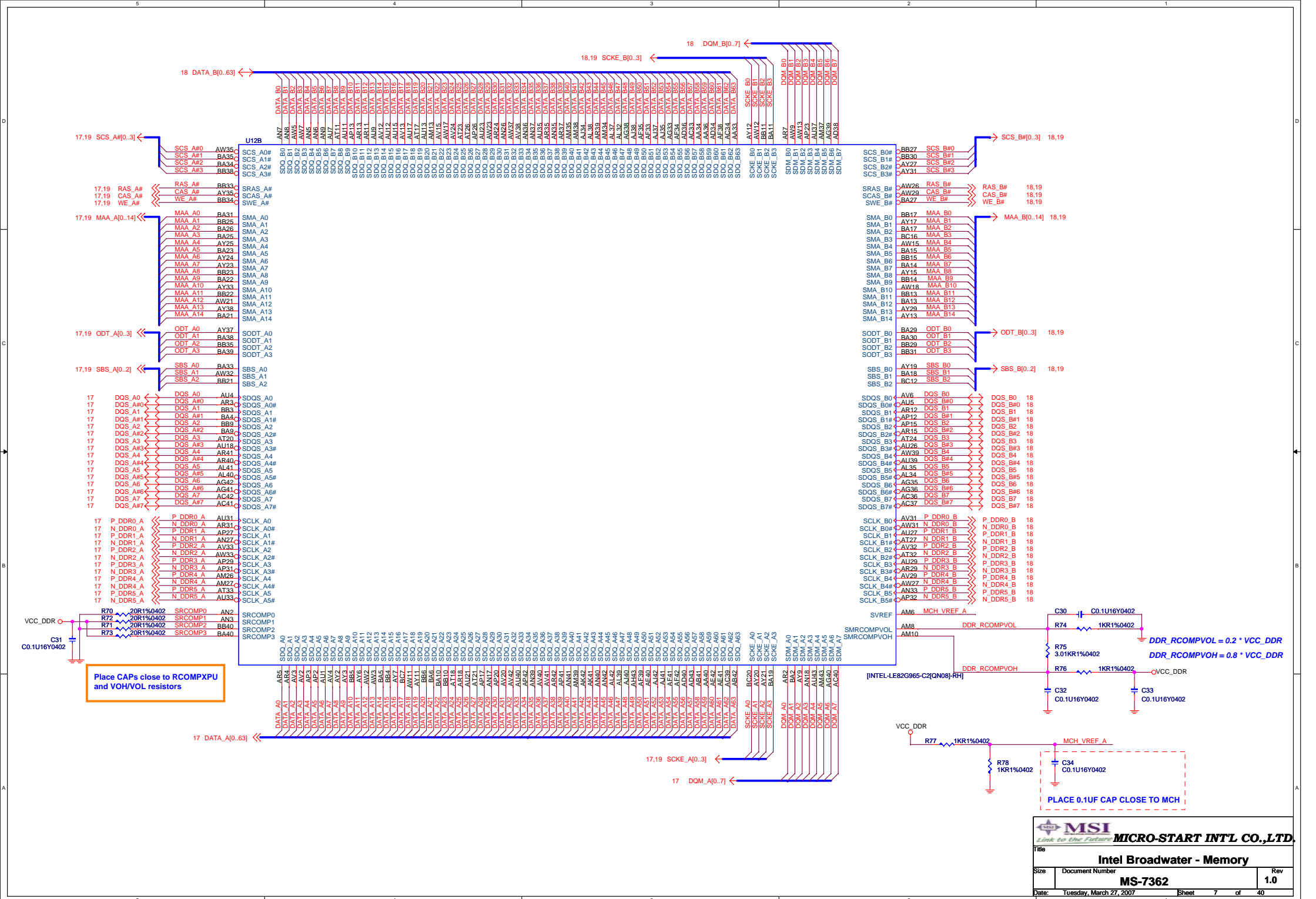
Intel LGA775 CPU - Signals

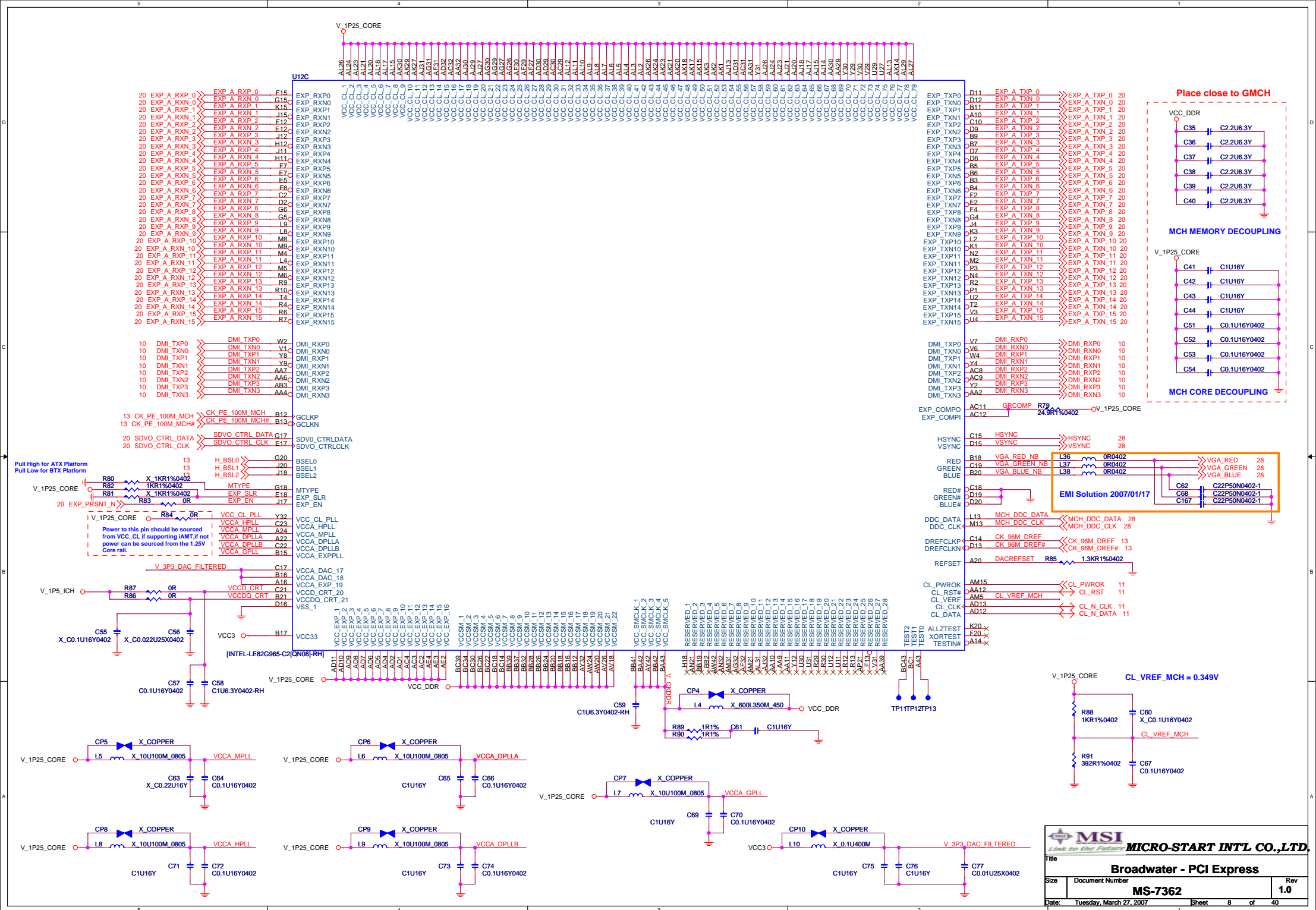


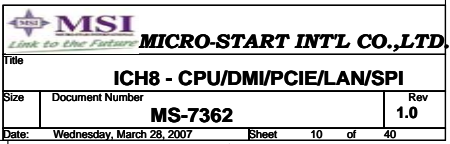


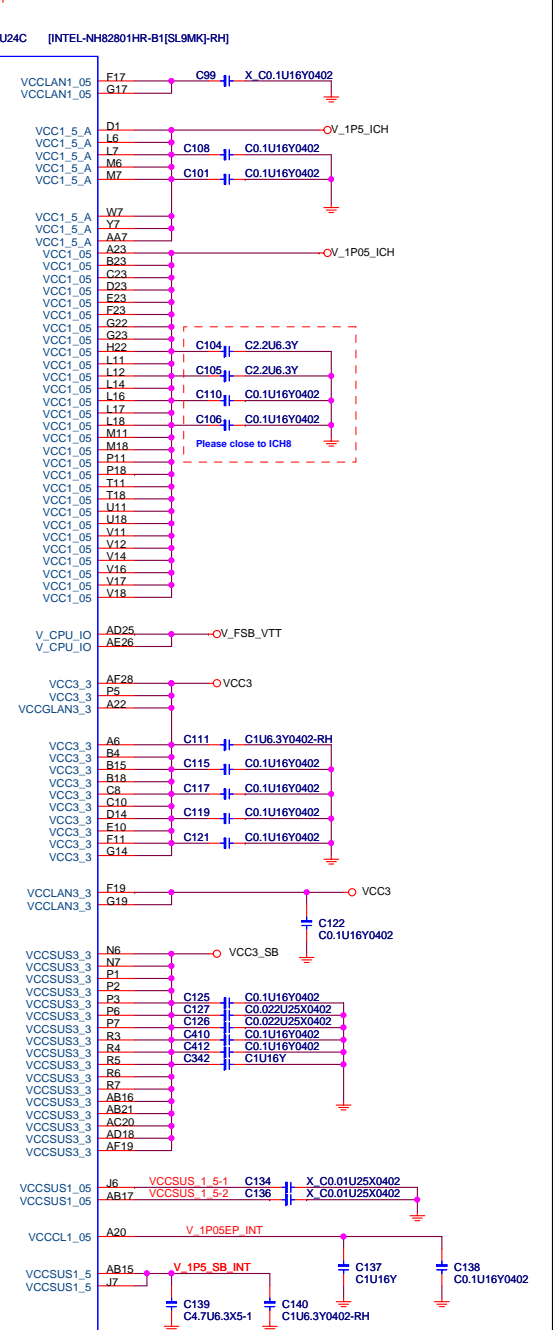
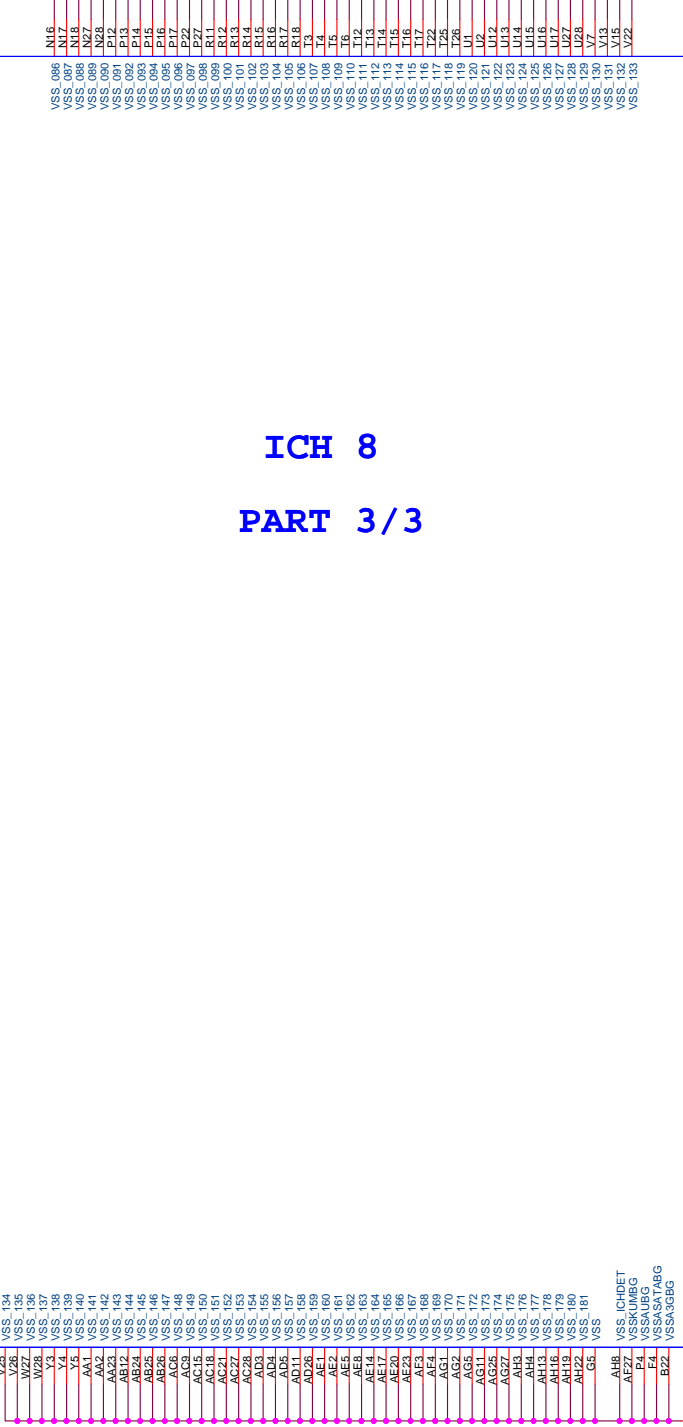
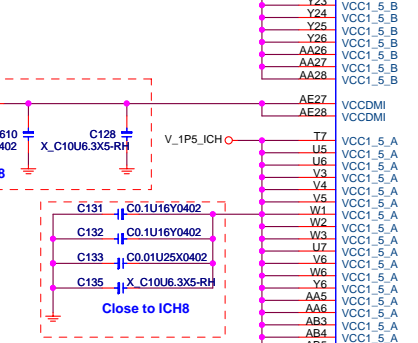
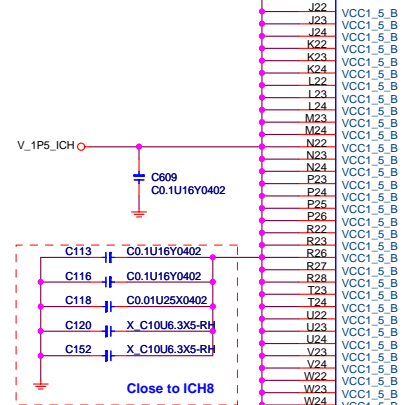
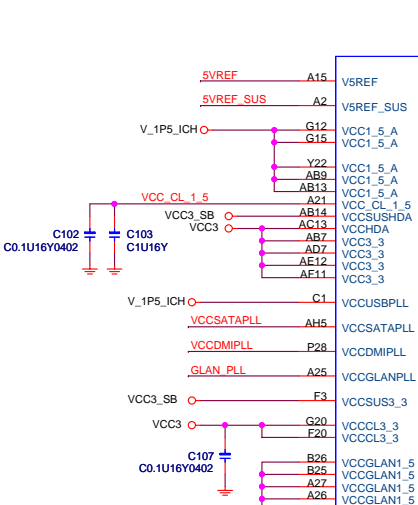
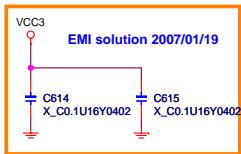
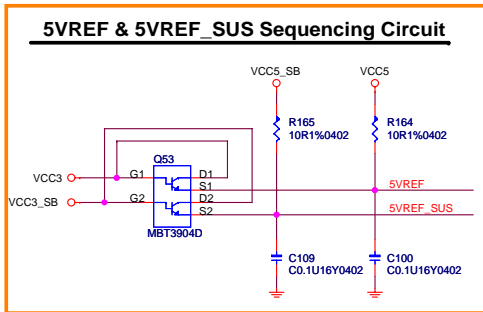
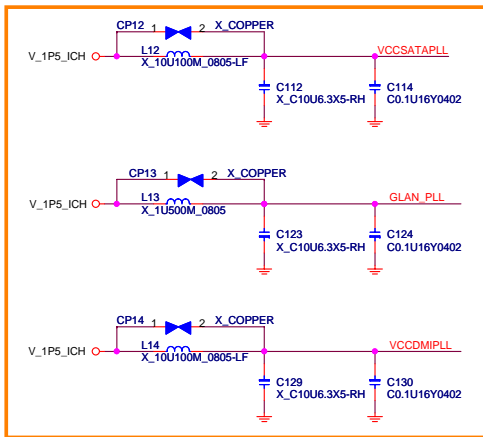




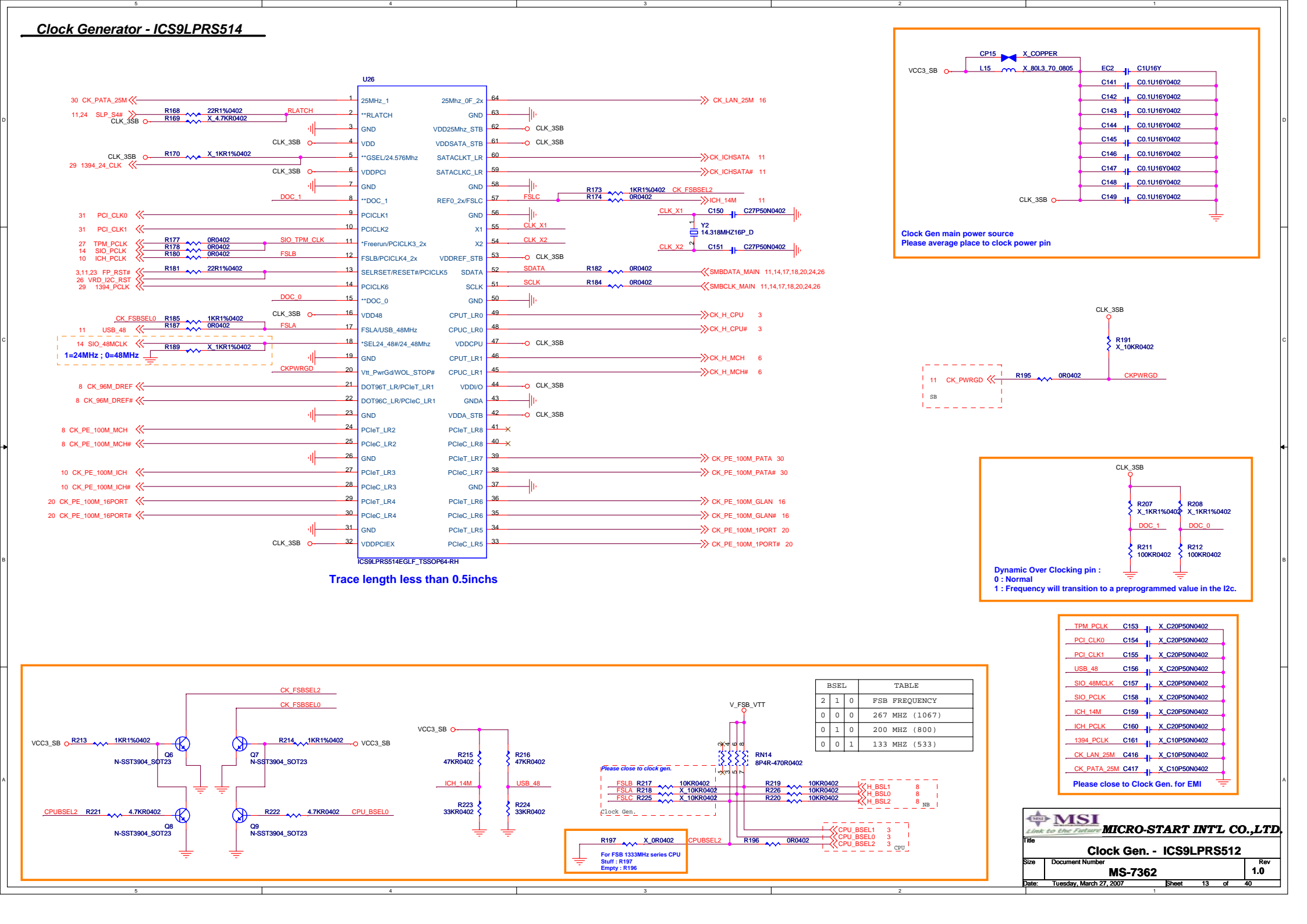
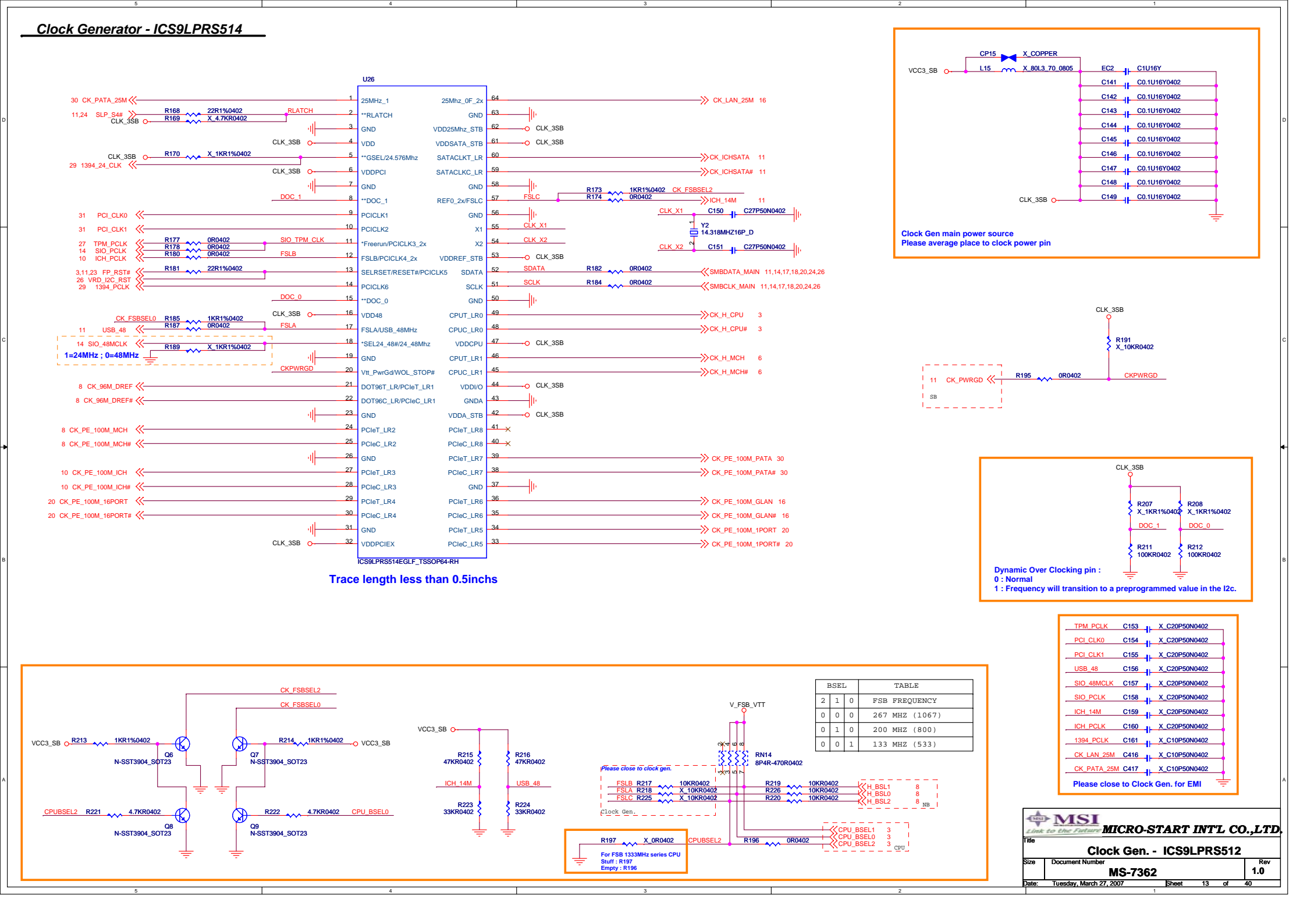
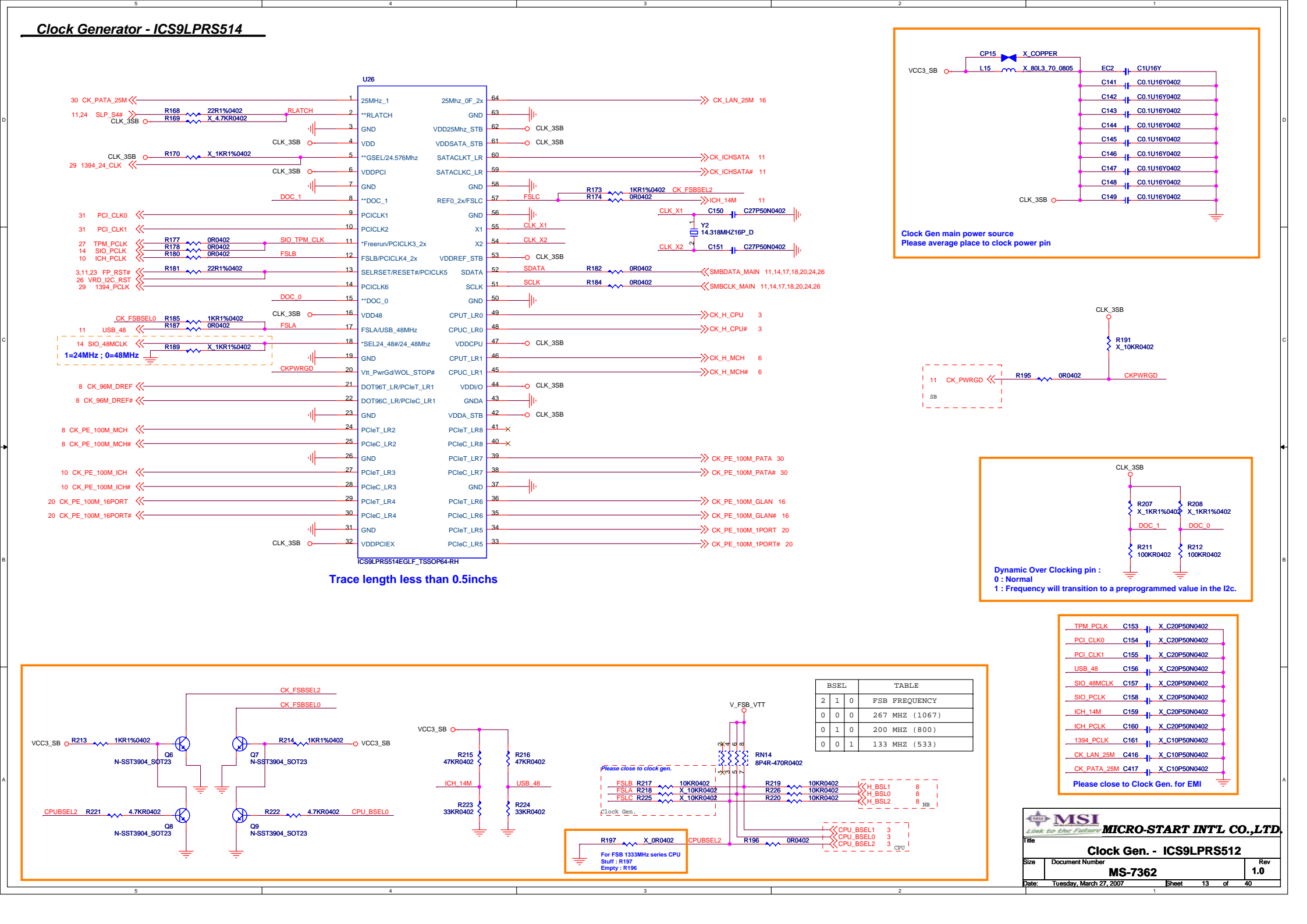
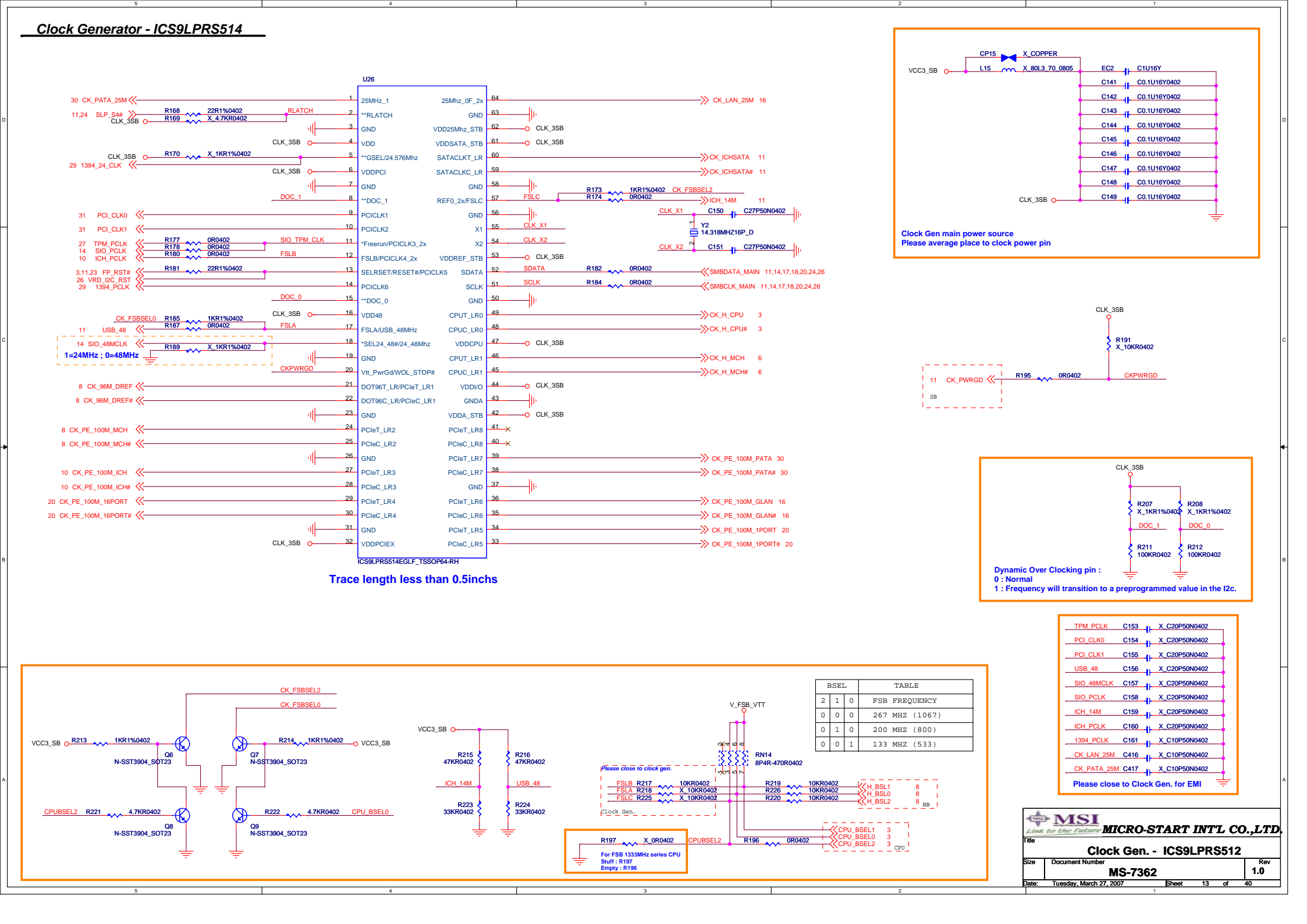








ICH 8
PART 3/3

[illegible]

Clock Generator - ICS9LPRS514

U26

30 CK_PATA_25M << 1 25MHz_1 64 >>> CK_LAN_25M 16

11.24 SLP_S4# >>> 2 **RLATCH 63 >>> GND

CLK_3SB <<< 3 GND 62 >>> CLK_3SB

29 1394_24_CLK <<< 4 VDD 61 >>> CLK_3SB

CLK_3SB <<< 5 **GSEL24.576Mhz 60 >>> CK_ICH_SATA 11

31 PCI_CLK0 <<< 6 VDDPCI 59 >>> CK_ICH_SATA# 11

31 PCI_CLK1 <<< 7 GND 58 >>> GND

27 TPM_PCLK <<< 8 **DOC_1 57 >>> ICH_14M 11

14 SIO_PCLK <<< 9 PCICLK1 56 >>> GND

10 ICH_PCLK <<< 10 PCICLK2 55 >>> CLK_X1

3.11.23 FP_RST# <<< 11 *Freerun/PCICLK3_2x 54 >>> CLK_X2

26 VRD_I2C_RST <<< 12 FSLB/PCICLK4_2x 53 >>> CLK_3SB

29 1394_PCLK <<< 13 SELRSET/RESET#/PCICLK5 52 >>> SDATA

11 USB_48 <<< 14 PCICLK6 51 >>> SCLK

14 SIO_48MCLK <<< 15 **DOC_0 50 >>> GND

1=24MHz; 0=48MHz <<< 16 VDD48 49 >>> CK_H_CPU 3

8 CK_96M_DREF <<< 17 FSLA/USB_48MHz 48 >>> CK_H_CPU# 3

8 CK_96M_DREF# <<< 18 *SEL24_48#/24_48MHz 47 >>> CLK_3SB

8 CK_PE_100M_MCH <<< 19 GND 46 >>> CK_H_MCH 6

8 CK_PE_100M_MCH# <<< 20 CKPWGRD 45 >>> CK_H_MCH# 6

10 CK_PE_100M_ICH <<< 21 DOT96T_LR/PCIE_T_LR1 44 >>> CLK_3SB

10 CK_PE_100M_ICH# <<< 22 DOT96C_LR/PCIE_C_LR1 43 >>> GND

20 CK_PE_100M_16PORT <<< 23 GND 42 >>> CLK_3SB

20 CK_PE_100M_16PORT# <<< 24 PCIE_T_LR2 41 >>> CK_PE_100M_PATA 30

20 CK_PE_100M_16PORT# <<< 25 PCIE_C_LR2 40 >>> CK_PE_100M_PATA# 30

20 CK_PE_100M_16PORT# <<< 26 GND 39 >>> CK_PE_100M_PATA 30

20 CK_PE_100M_16PORT# <<< 27 PCIE_T_LR3 38 >>> CK_PE_100M_PATA# 30

20 CK_PE_100M_16PORT# <<< 28 PCIE_C_LR3 37 >>> GND

20 CK_PE_100M_16PORT# <<< 29 PCIE_T_LR4 36 >>> CK_PE_100M_GLAN 16

20 CK_PE_100M_16PORT# <<< 30 PCIE_C_LR4 35 >>> CK_PE_100M_GLAN# 16

20 CK_PE_100M_16PORT# <<< 31 GND 34 >>> CK_PE_100M_1PORT 20

20 CK_PE_100M_16PORT# <<< 32 PCIE_T_LR5 33 >>> CK_PE_100M_1PORT# 20

20 CK_PE_100M_16PORT# <<< 33 PCIE_C_LR5 33 >>> CK_PE_100M_1PORT# 20

ICS9LPRS514EGLF-TSSOP64-RH

Trace length less than 0.5inches

CK_FSBSEL2

CK_FSBSEL0

VCC3_SB

R213 1KR1%0402

Q6 N-SST3904_SOT23

Q7 N-SST3904_SOT23

R214 1KR1%0402

VCC3_SB

CPUBSEL2 R221 4.7KR0402

Q8 N-SST3904_SOT23

Q9 N-SST3904_SOT23

R222 4.7KR0402

CPU_BSEL0

VCC3_SB

R215 47KR0402

R216 47KR0402

ICH_14M

R223 33KR0402

R224 33KR0402

V_FSB_VTT

8P4R-470R0402

RN14

R219 10KR0402

R220 10KR0402

R221 10KR0402

R222 10KR0402

R223 10KR0402

R224 10KR0402

R225 10KR0402

R226 10KR0402

R227 10KR0402

R228 10KR0402

R229 10KR0402

R230 10KR0402

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R334 10KR0402

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R336 10KR0402

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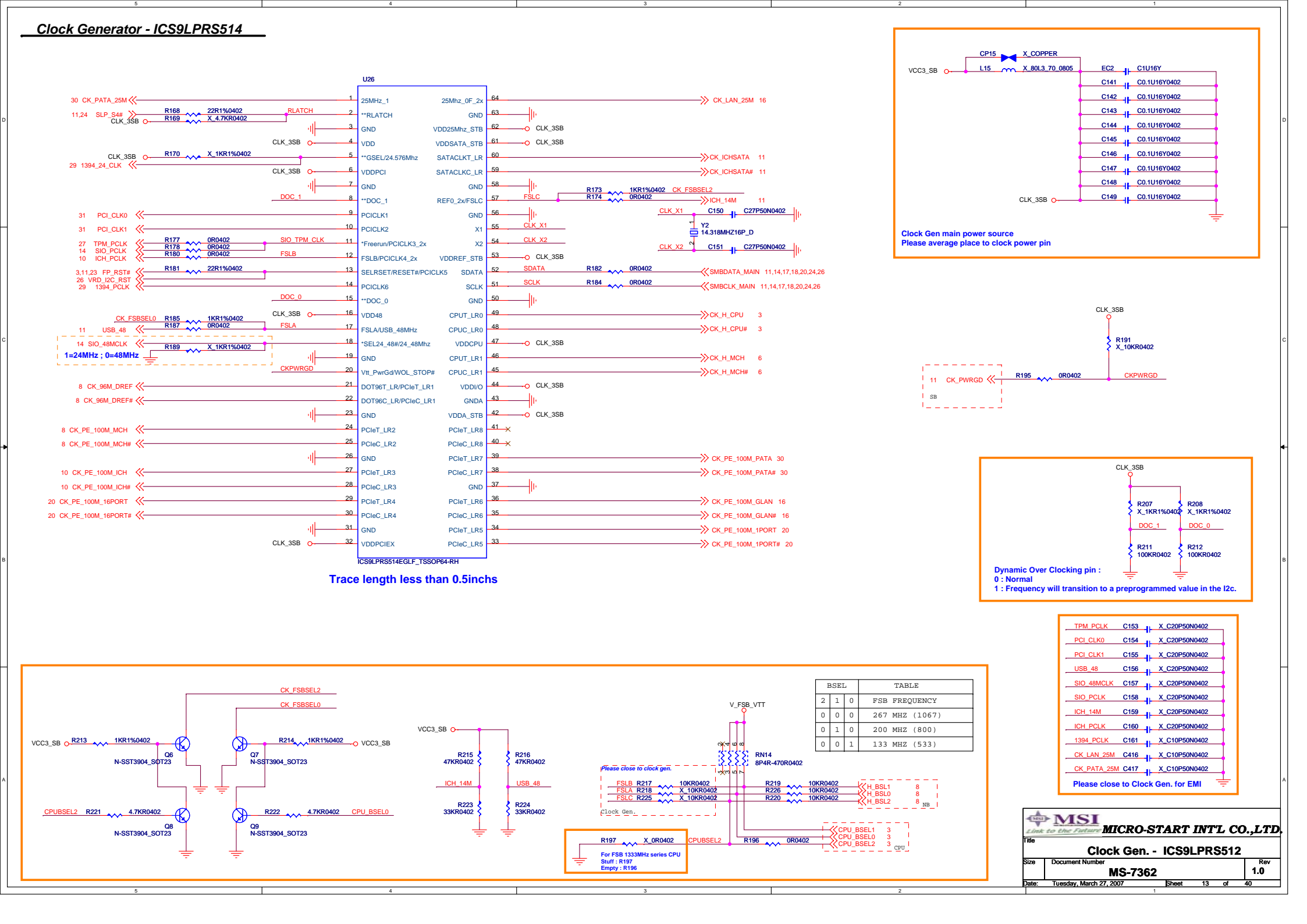
R349 10KR0402

R350 10KR0402

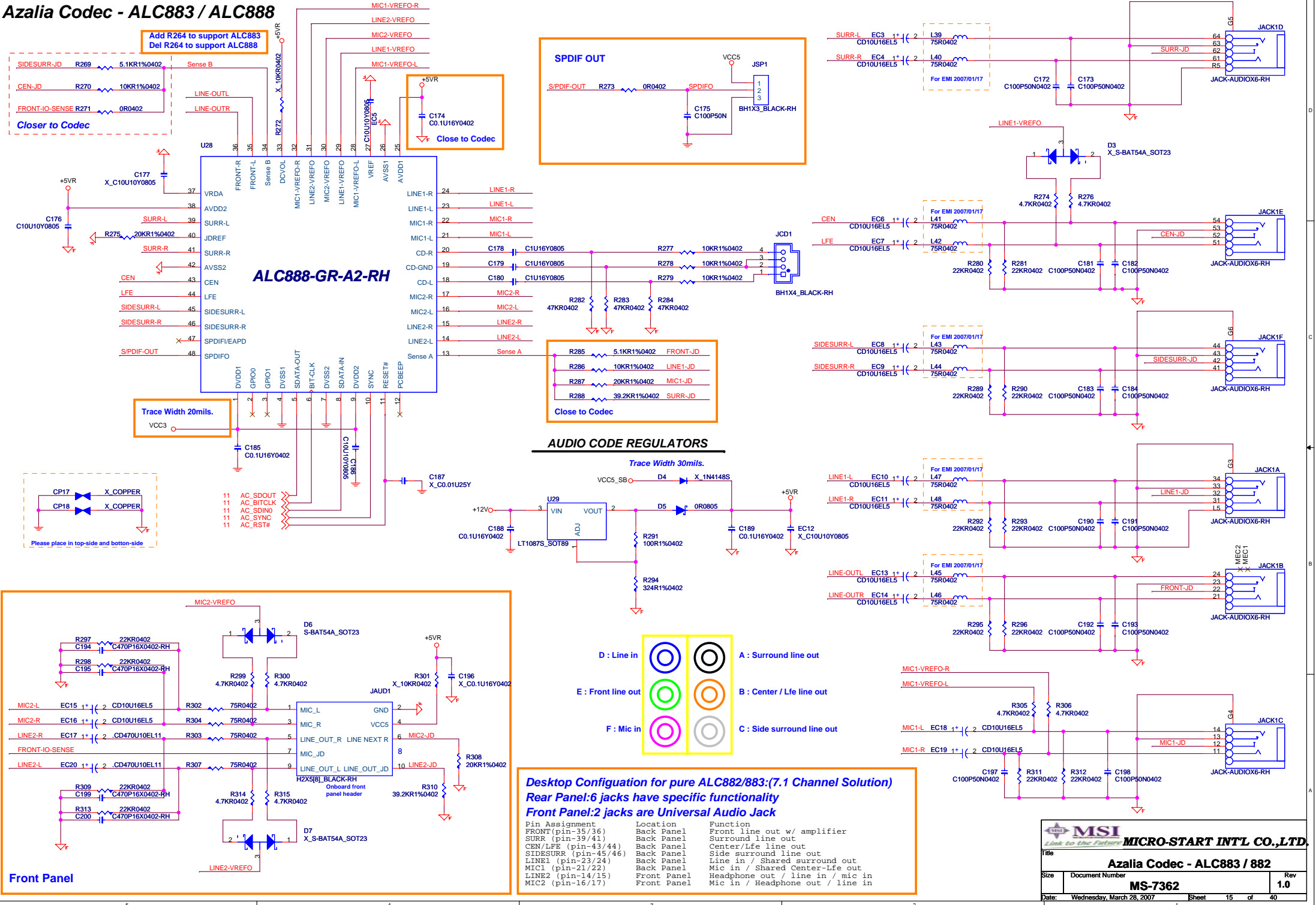
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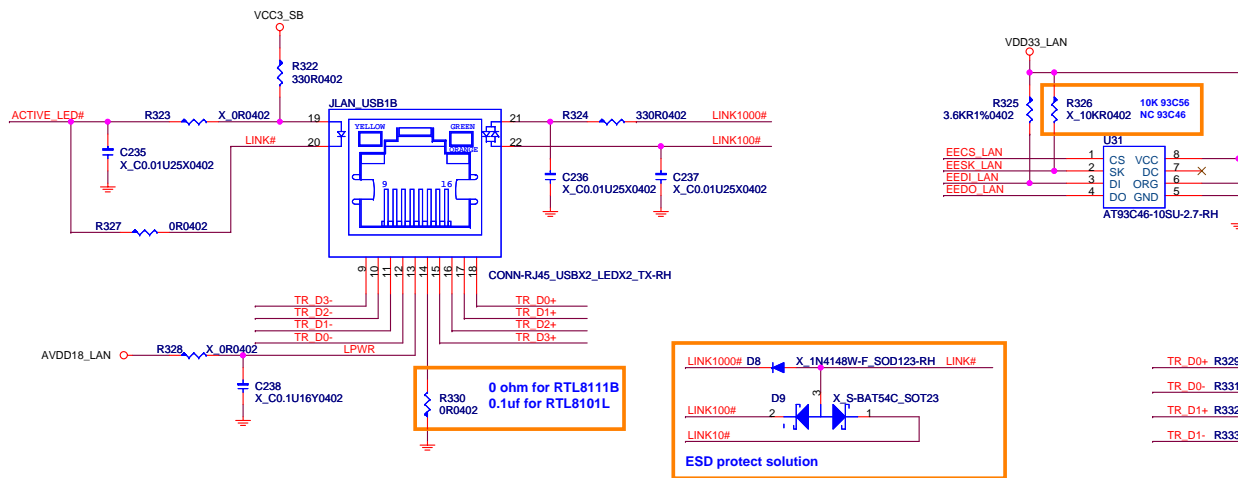
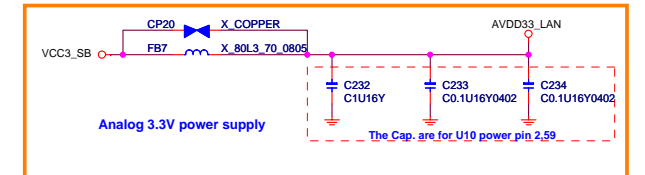
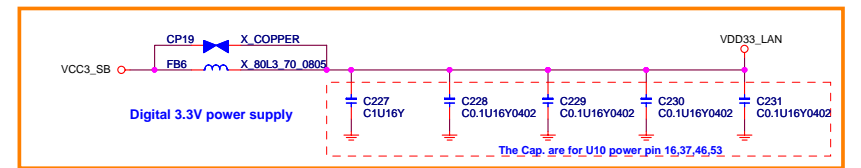
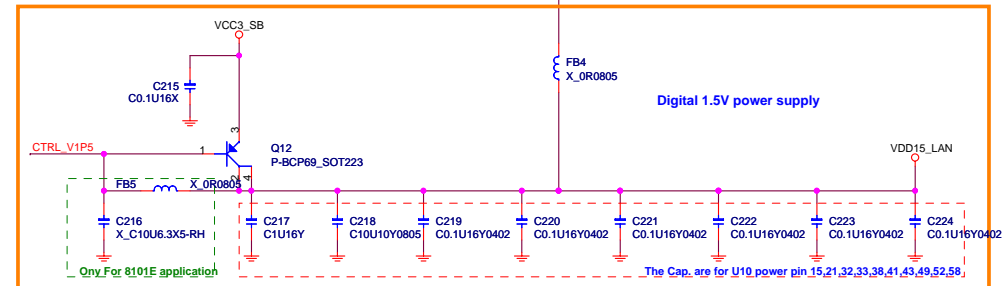
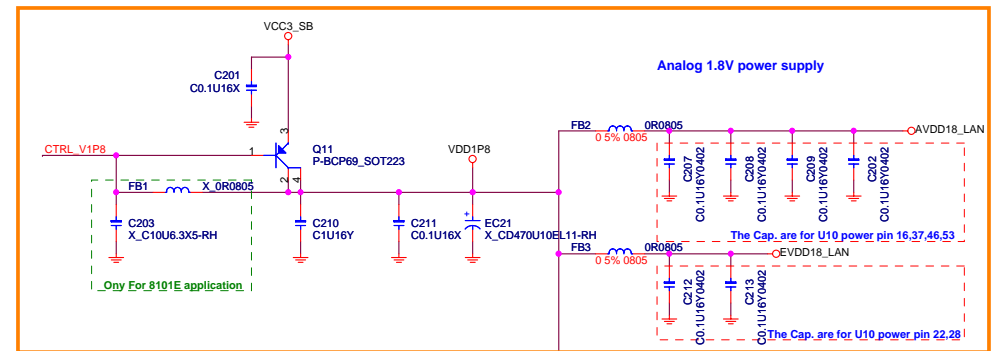
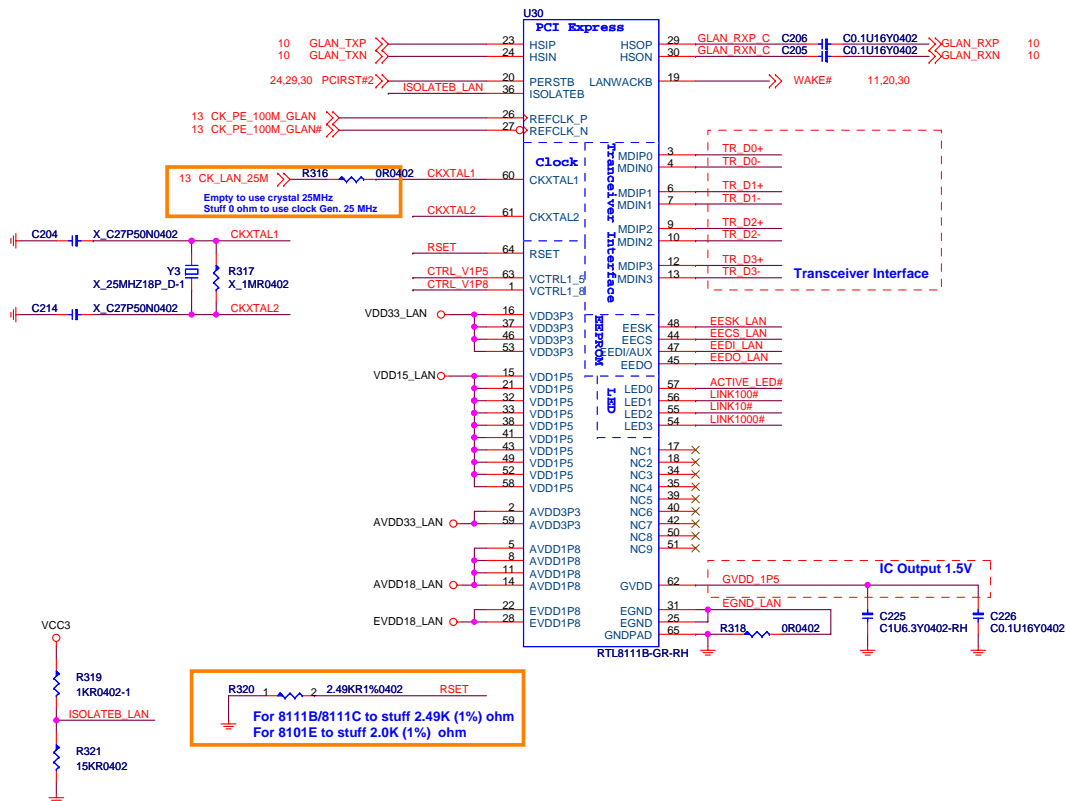
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R



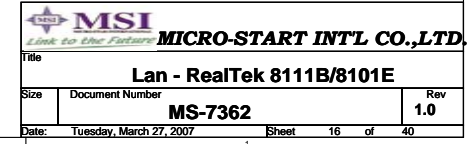
Azalia Codec - ALC883 / ALC888



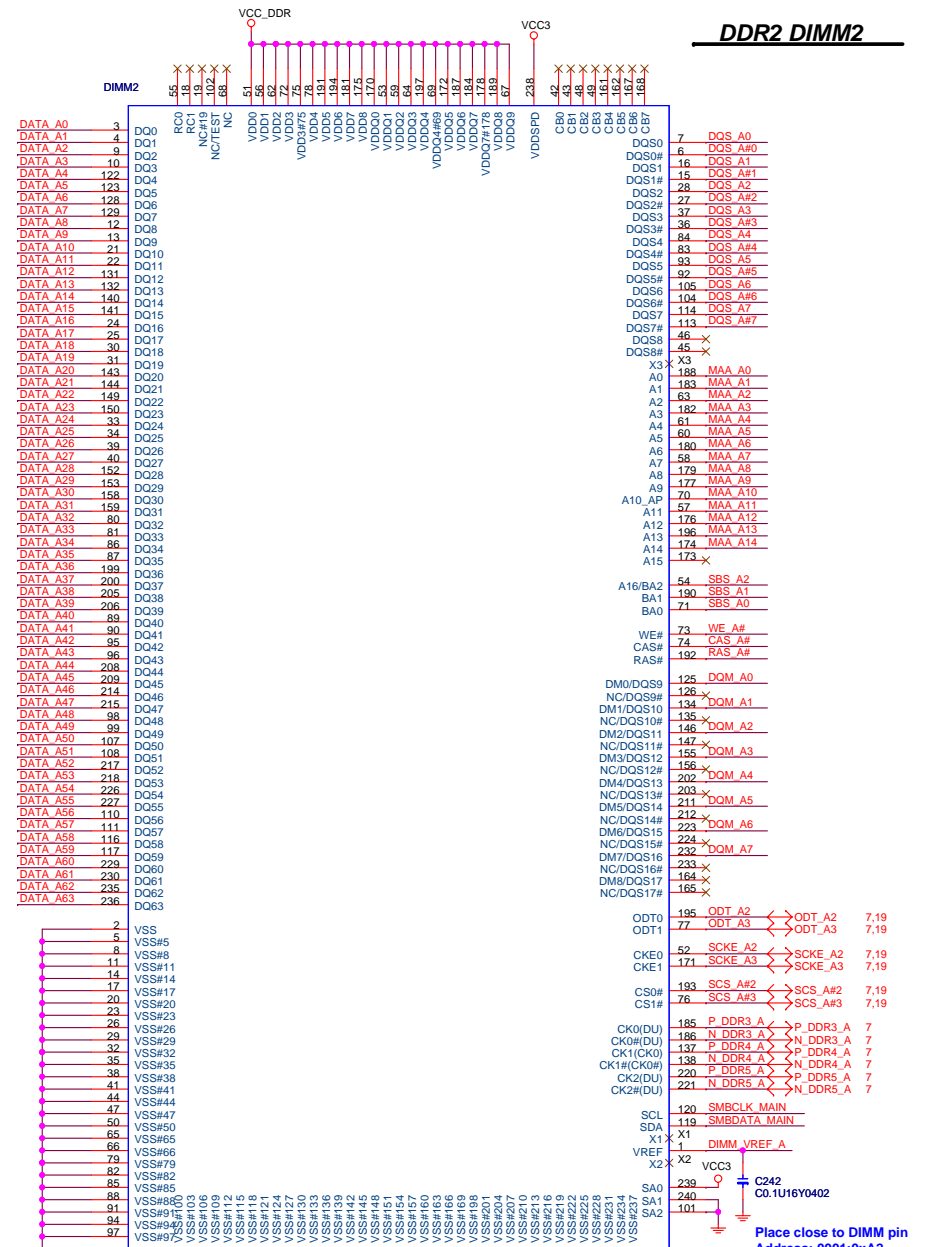
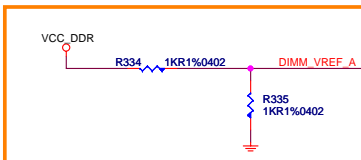
RealTek - RTL8111B-GR / RTL8101E-GR

Power Domain Chart

	RTL8111B	RTL8101E	RTL8111C
AVDD33	3.3V	3.3V	3.3V
AVDD18	1.8V	1.8V	1.2V
EVDD18	1.8V	1.8V	1.2V
DVDD15	1.5V	1.5V	1.2V
Q1	Need	N/A	N/A
Q2	Need	N/A	N/A



CHANNEL A



MSI
Link to the Future

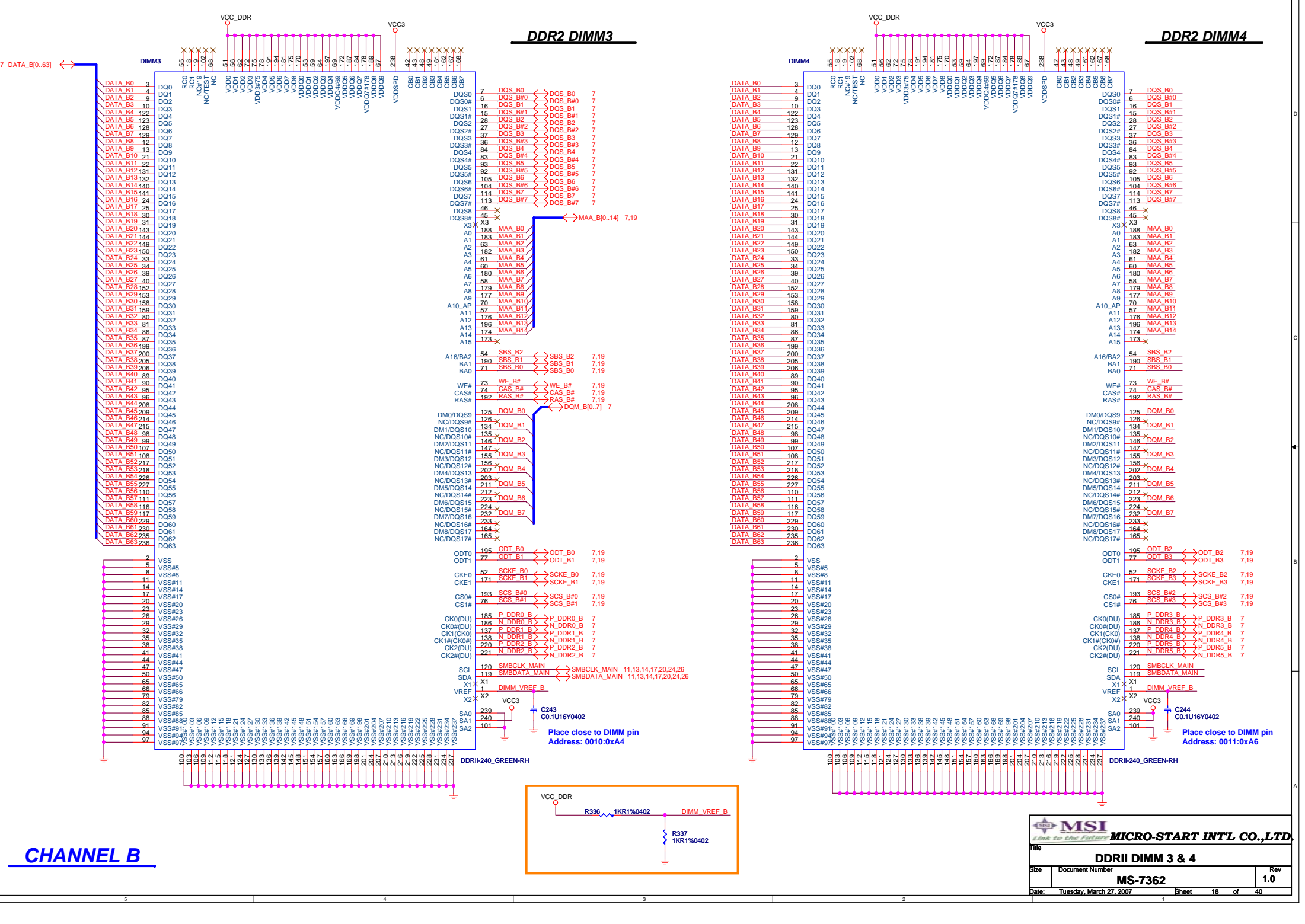
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DDR2 DIMM 1 & 2

Size: Document Number
Rev: 1.0

Date: Tuesday, March 27, 2007 Sheet 17 of 40

CHANNEL B



MSI
Link to the Future

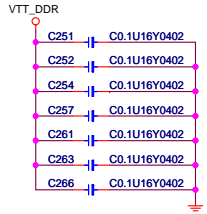
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DDR2 DIMM 3 & 4

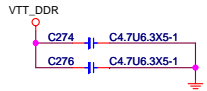
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MS-7362
Rev: 1.0

Date: Tuesday, March 27, 2007 Sheet 18 of 40

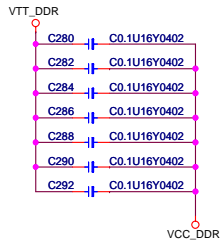
CHANNEL A V_SM_VTT
DECOUPLING CAPS



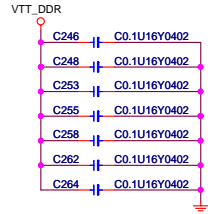
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VTT ISLAND



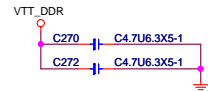
CHANNEL A ADDRESS/CONTROL
STITCHING CAPS



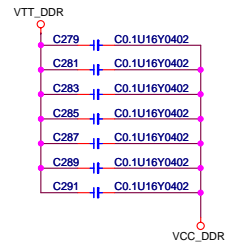
CHANNEL B V_SM_VTT
DECOUPLING CAPS



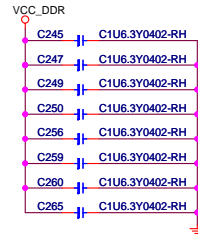
PLACED AT LEFT AND
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VTT ISLAND



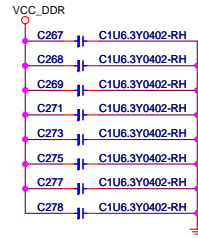
CHANNEL B ADDRESS/CONTROL
STITCHING CAPS



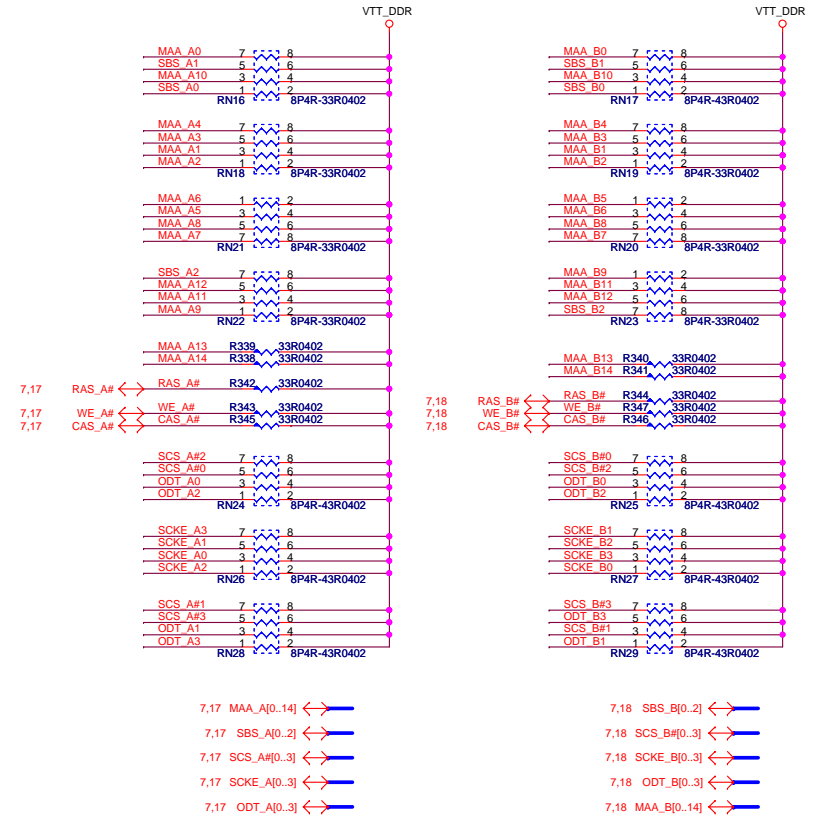
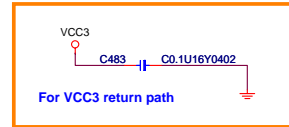
Close to DIMM slot
as possible



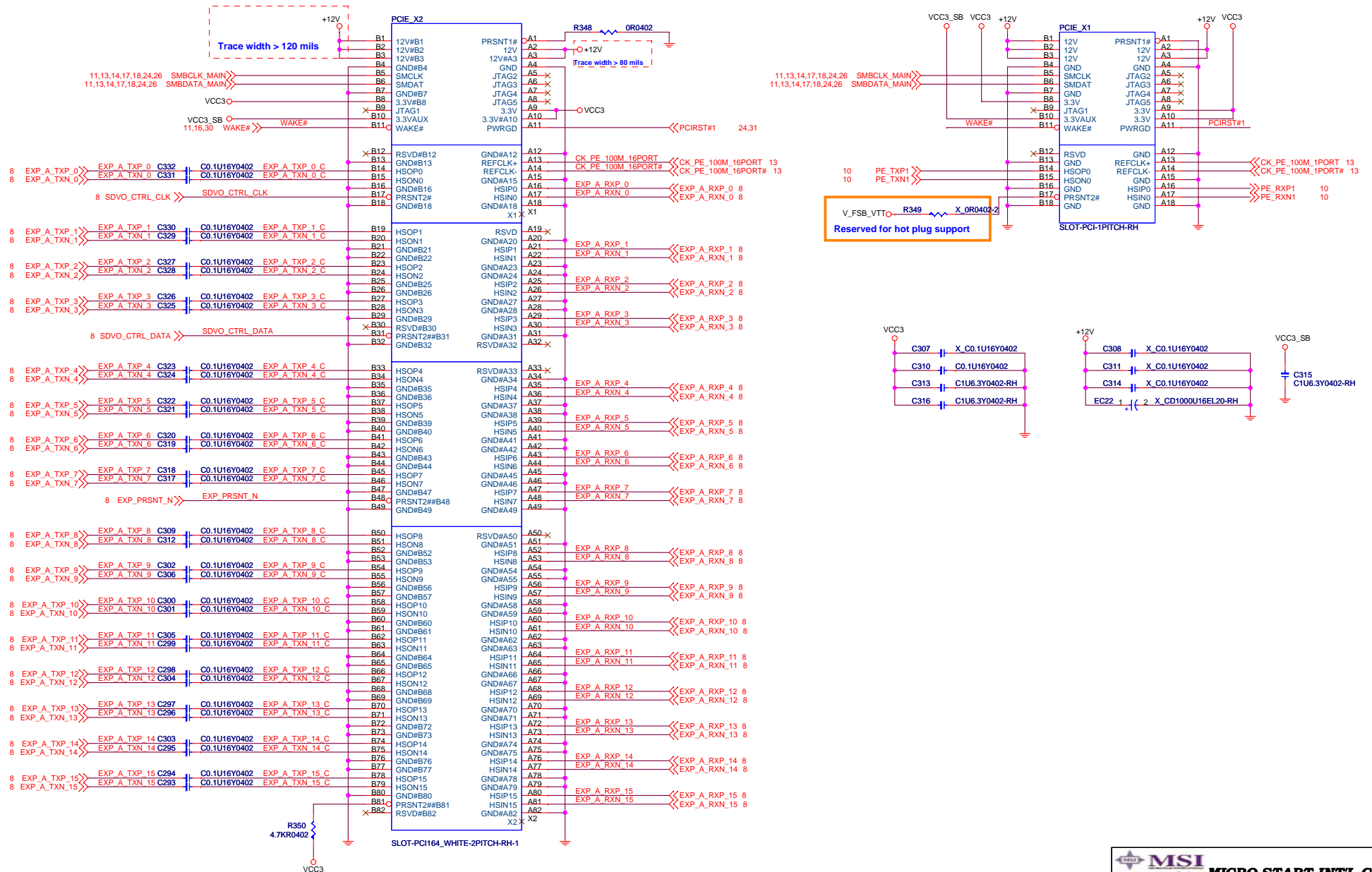
Close to DIMM slot
as possible



Close to DIMM slot
as possible



PCI Express x 16 & x 1 Slot



[illegible]

The schematic diagram illustrates the internal circuitry of the H2X5(10)_white-RH module. Key components include the U33 IC (AZ75232SGSTR-E1_SSOP20-RH) and two X_8P4C-180P50N capacitors (CN7 and CN8). The module's pins are connected to a +12V and -12V power supply through diodes D13 and D14, and capacitors C343 and C346. The module is also connected to a COM2 header with pins 1 through 8.

Module Pin Connections:

- NR1B# (Pin 1) to NR1B# (Pin 14)
- NCTSB# (Pin 2) to NCTSB# (Pin 14)
- NDSRB# (Pin 3) to NDSRB# (Pin 14)
- NSINB# (Pin 4) to NSINB# (Pin 14)
- NDCDB# (Pin 5) to NDCDB# (Pin 14)
- RTSB# (Pin 6) to RTSB# (Pin 14)
- DTRB# (Pin 7) to DTRB# (Pin 14)
- SOUTB# (Pin 8) to SOUTB# (Pin 14)
- NRTSB# (Pin 9) to NRTSB# (Pin 14)
- NDRTRB# (Pin 10) to NDRTRB# (Pin 14)
- NSOUTB# (Pin 11) to NSOUTB# (Pin 14)
- NDSRB# (Pin 12) to NDSRB# (Pin 14)

Internal Connections:

- VCC5 to VCC (Pin 20)
- VCC (Pin 20) to VCC (Pin 1)
- VCC (Pin 20) to VCC (Pin 19)
- VCC (Pin 20) to VCC (Pin 18)
- VCC (Pin 20) to VCC (Pin 17)
- VCC (Pin 20) to VCC (Pin 16)
- VCC (Pin 20) to VCC (Pin 15)
- VCC (Pin 20) to VCC (Pin 14)
- VCC (Pin 20) to VCC (Pin 13)
- VCC (Pin 20) to VCC (Pin 12)
- VCC (Pin 20) to VCC (Pin 11)
- VCC (Pin 20) to VCC (Pin 10)
- VCC (Pin 20) to VCC (Pin 9)
- VCC (Pin 20) to VCC (Pin 8)
- VCC (Pin 20) to VCC (Pin 7)
- VCC (Pin 20) to VCC (Pin 6)
- VCC (Pin 20) to VCC (Pin 5)
- VCC (Pin 20) to VCC (Pin 4)
- VCC (Pin 20) to VCC (Pin 3)
- VCC (Pin 20) to VCC (Pin 2)
- VCC (Pin 20) to VCC (Pin 1)

Capacitor Connections:


- CN7 (X_8P4C-180P50N) connected to pins 1, 2, 3, 4, 5, 6, 7, 8
- CN8 (X_8P4C-180P50N) connected to pins 1, 2, 3, 4, 5, 6, 7, 8

Power Supply Connections:

- +12V to D13 (1N4148S) to C343 (C0.1U16Y0402) to VCC (Pin 20)
- 12V to D14 (1N4148S) to C346 (C0.1U16Y0402) to VCC (Pin 20)

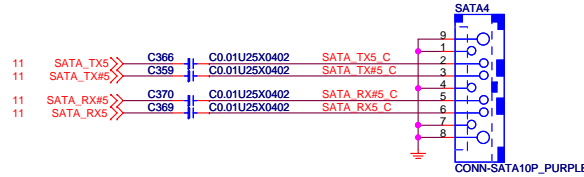
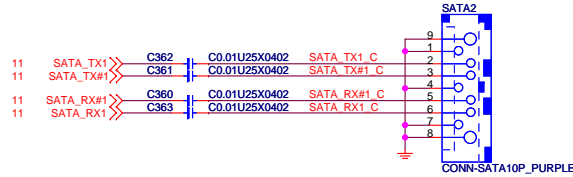
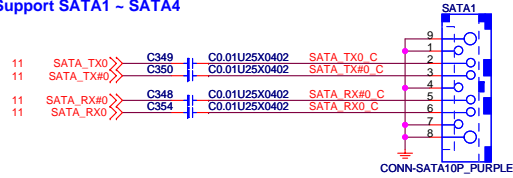
COM2 Header Connections:

- COM2 (Pin 1) to NR1B# (Pin 1)
- COM2 (Pin 2) to NCTSB# (Pin 2)
- COM2 (Pin 3) to NDSRB# (Pin 3)
- COM2 (Pin 4) to NSINB# (Pin 4)
- COM2 (Pin 5) to NDCDB# (Pin 5)
- COM2 (Pin 6) to RTSB# (Pin 6)
- COM2 (Pin 7) to DTRB# (Pin 7)
- COM2 (Pin 8) to SOUTB# (Pin 8)

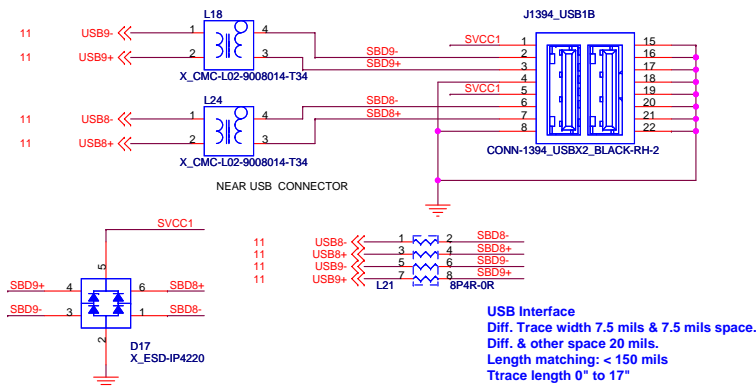
 MSI <i>Link to the Future</i>				MICRO-START INT'L CO.,LTD.			
Title LPT / COM / KB / MS							
Size		Document Number MS-7362				Rev 1.0	
Date		Tuesday, March 27, 2007		Sheet		21 of 40	

Serial ATA Connector and USB Connector

ICH8R Support SATA1 ~ SATA6
ICH8 Only Support SATA1 ~ SATA4

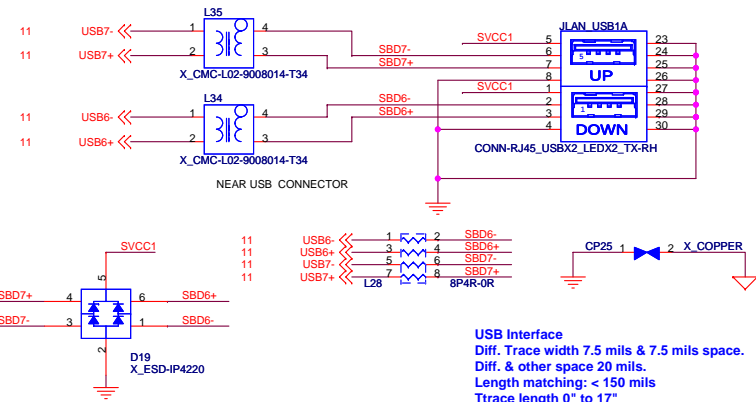


REAR PANEL USB CONNECTOR FOR USB PORT 8,9



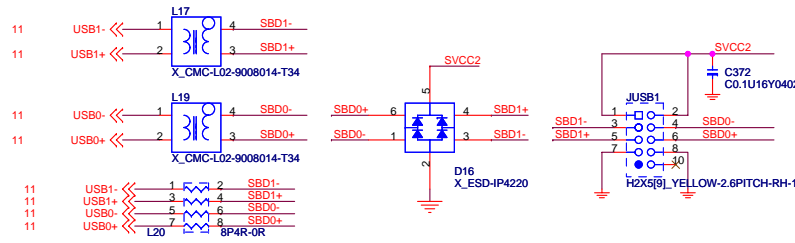
USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Ttrace length 0" to 17"

REAR PANEL USB CONNECTOR FOR USB PORT 6,7

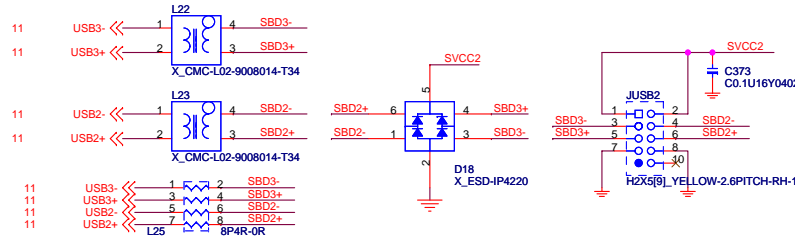


USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Ttrace length 0" to 17"

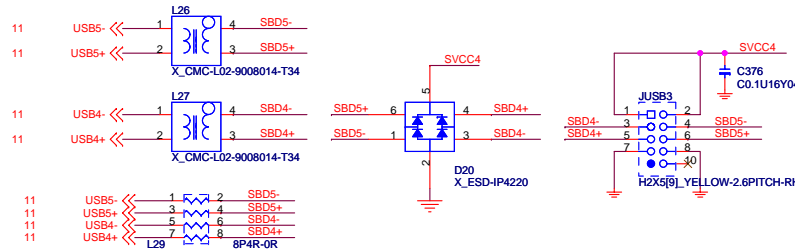
FRONT PANEL USB CONNECTOR FOR USB PORT 0,1



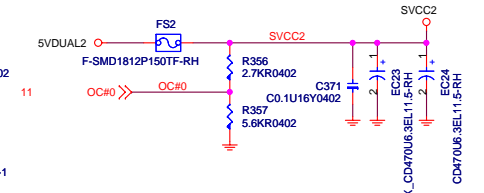
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



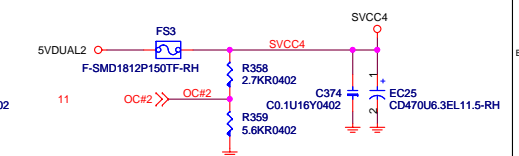
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



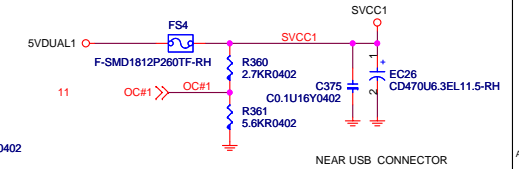
POWER CIRCUIT FOR USB PORT 0,1,2,3 (FRONT)



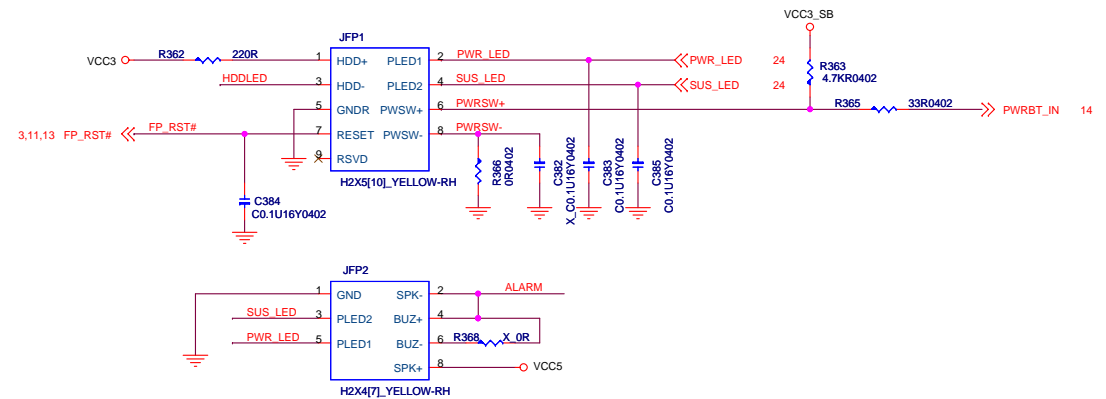
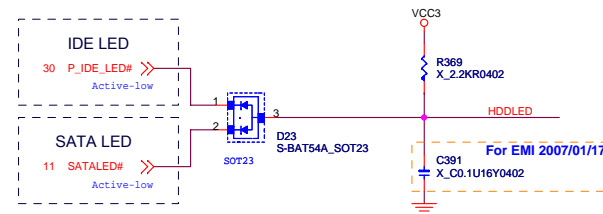
POWER CIRCUIT FOR USB PORT 4,5 (FRONT)



POWER CIRCUIT FOR USB PORT 6,7,8,9 (REAR)



Intel Front Panel

**HDD LED**

$$16.92W + 6.714W + 1.08W + 7.2W + 3.3W + 2.1W = 37.314W$$

$$37.314 / 1.8 = 20.73A$$

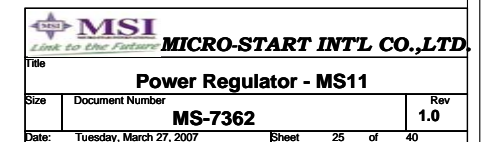
$$20.13 \times 1.15 = 23.84A$$


$$1.5 \times 2.2 + 2.1 = 5.4$$
$$5.4 / 1.5 = 3.6$$

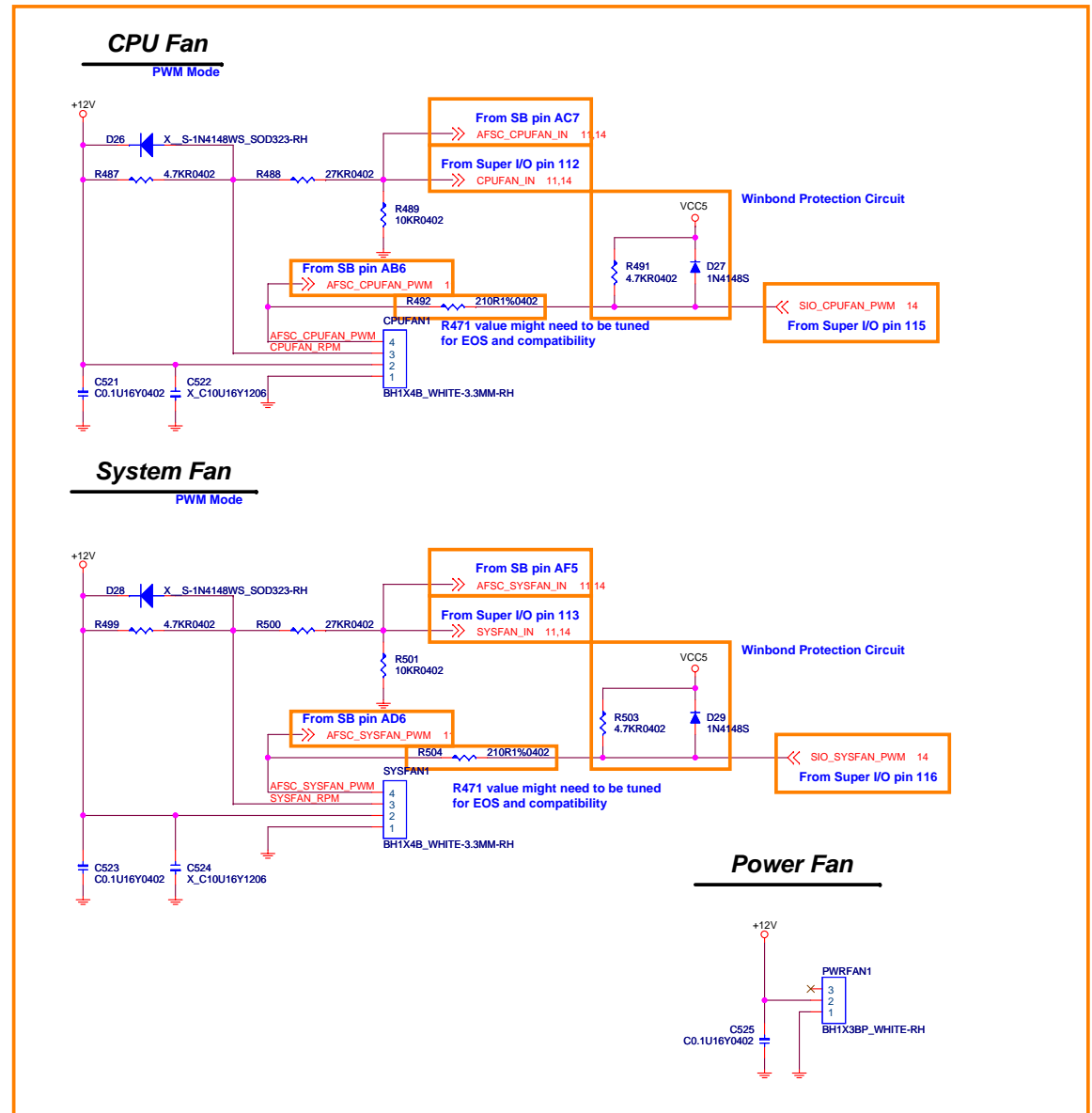
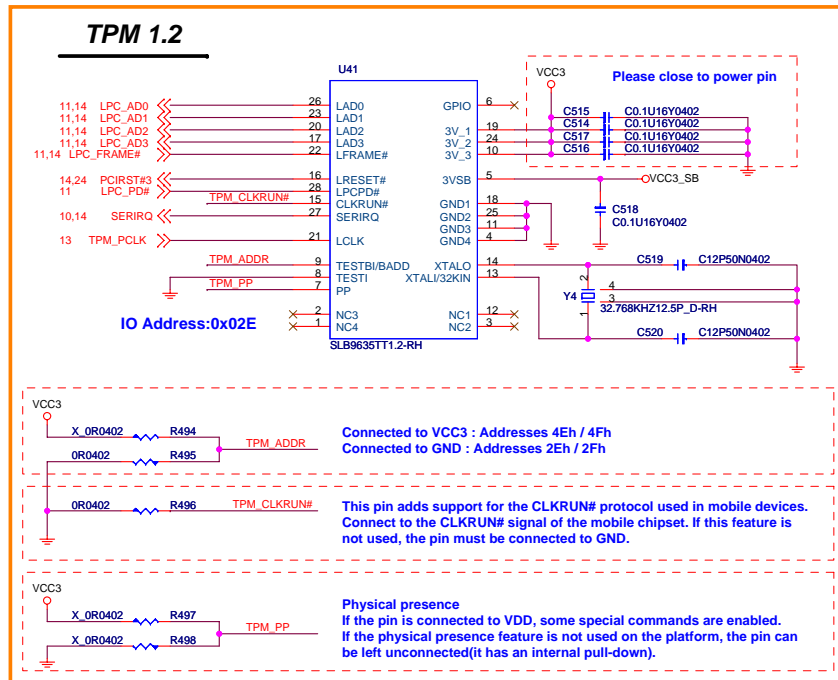
Liner Solution
D03-0903BDB-N03
,DIS MOSFET-N,NIKO/P0903BDG,TO252,50A,25V,+/-20V,9.5mohm(10V/25A),1V,,3V,1800pF,,50nC,,RoHS COMPLIANCE



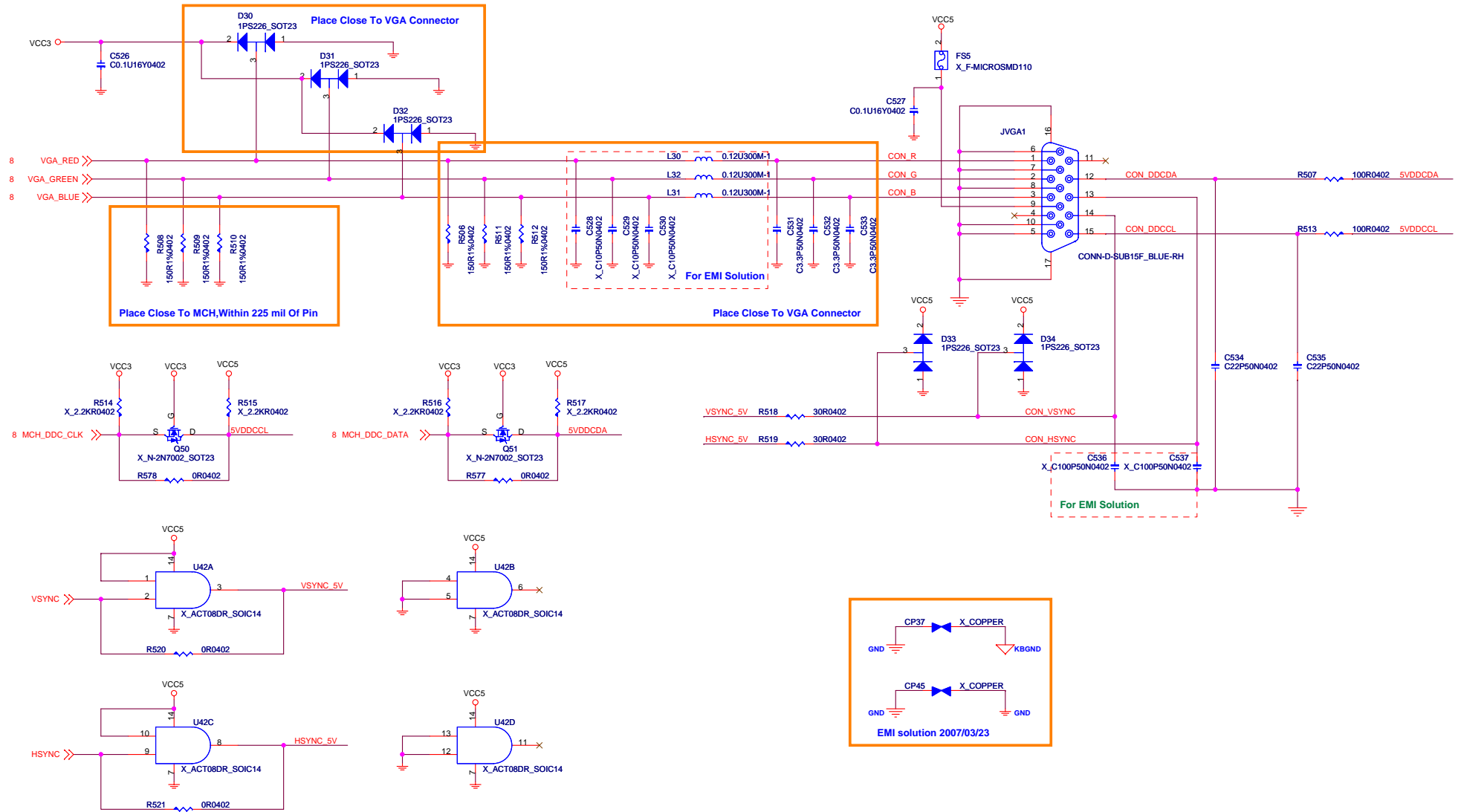
$$1.05 \times 2 = 2.1$$

[illegible]

TPM 1.2 / FAN Controller

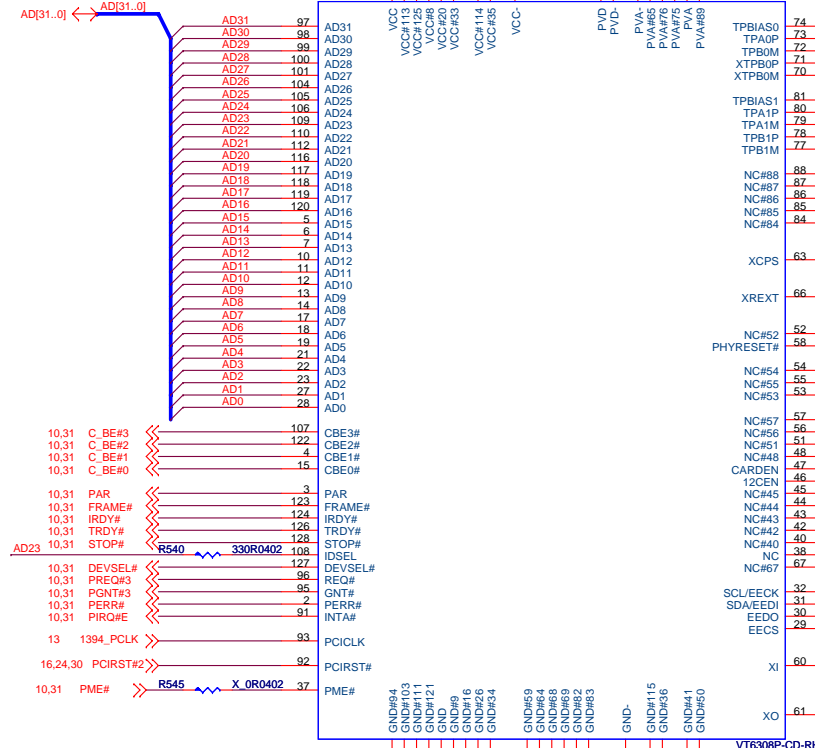
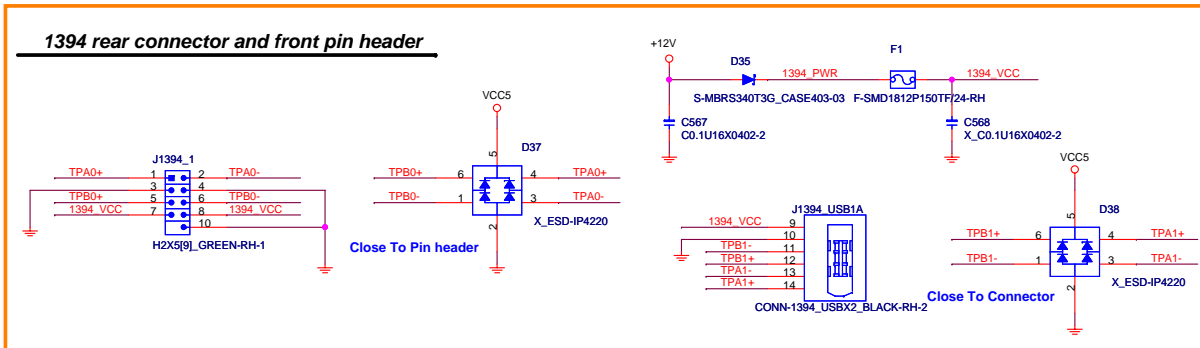
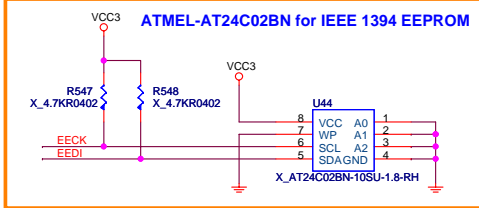
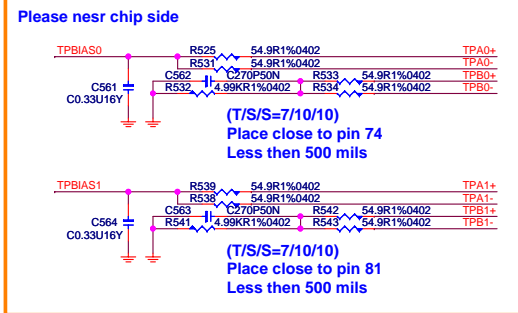
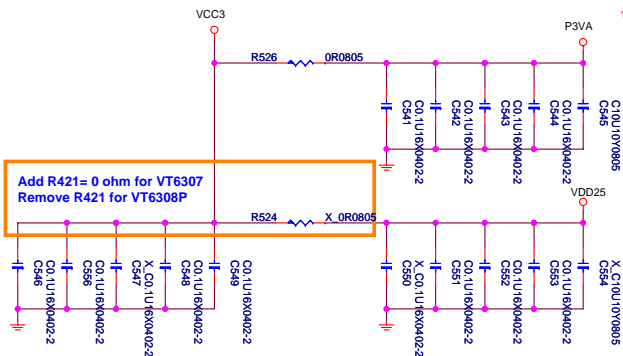
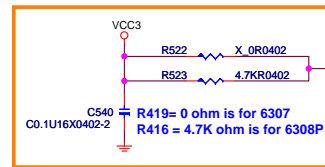


Video Connector

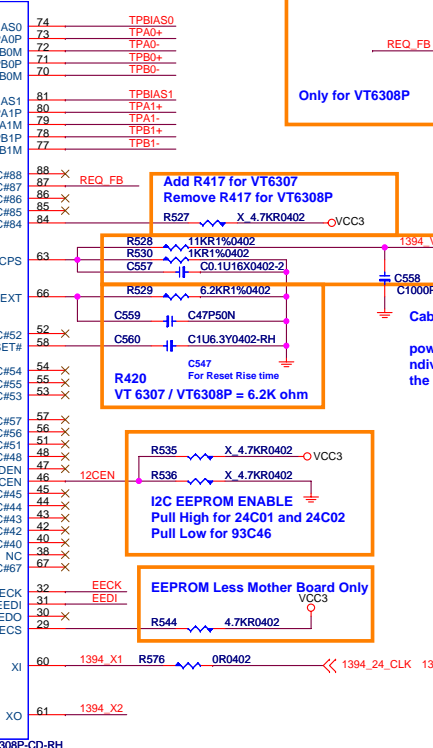


IEEE 1394 - VIA VT6307 / VT6308P

B07-6308P04-V01
 ,CHIP CONTROLLER,VIA/VT6308P,CD,PQFP-128pin,PCI 1394A-2000 INTEGRATED HOST CONTROLLER,RoHS COMPLIANCE
 B07-0630724-V01
 ,CHIP CONTROLLER,VIA/VT6307,CD,PQFP-128pin,PCI 1394A OHCI LINK LAYER WITH 2PORT PHY(14*20MM),RoHS COMPLIANCE

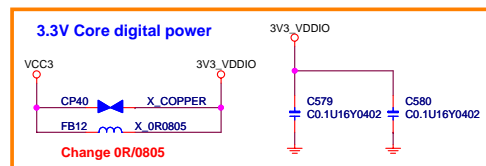
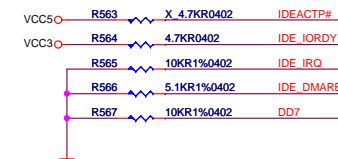
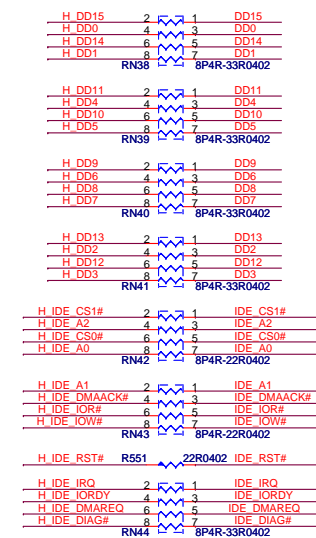
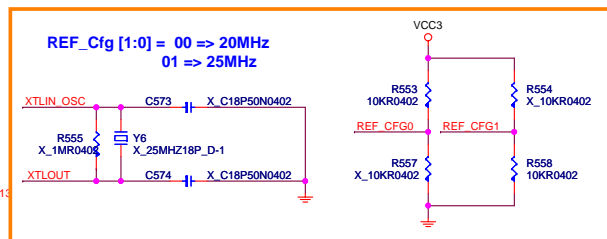
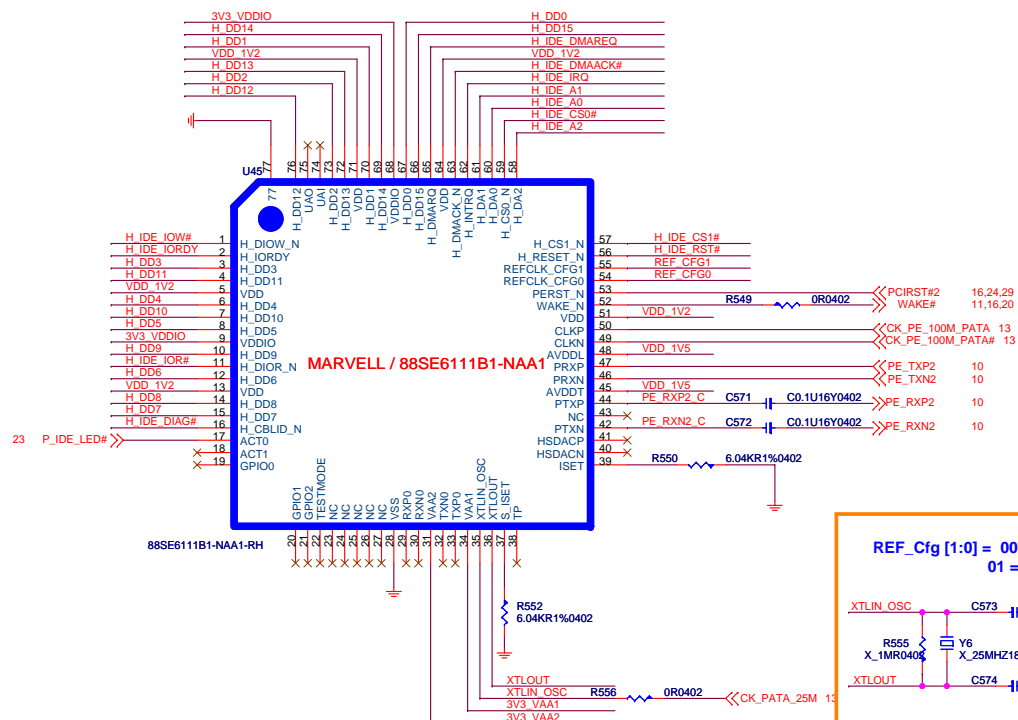


	U22	R422	R426
I2C EEPROM	24C02	4.7K ohm	Remove
No EEPROM	Remove	Remove	4.7K ohm

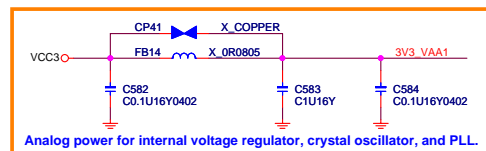


POWER Pin		
Pin	VT6307	VT6308P
84	NC	BJT_CTL
87	NC	REG_FB
88	NC	REQ_OUT
35	VCC3	PWRDET_VCC
39	VCC3	VCC3
49	VCC3	VDD
24	VCC3	VDD
114	VCC3	VDD
33	VCC3	VDD

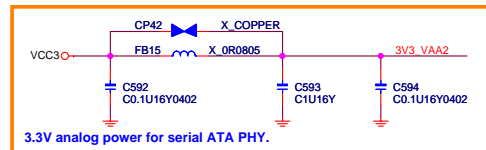
PCI Express To SATA / PATA Bridge



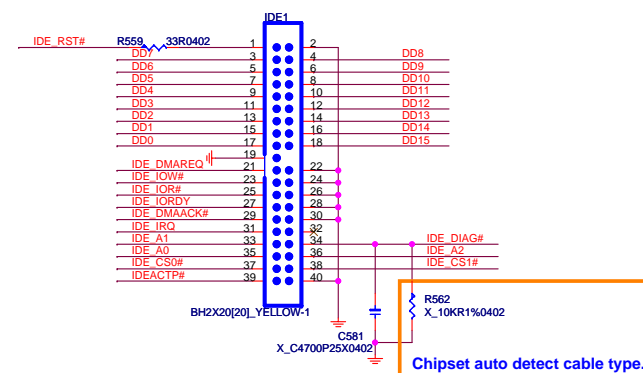
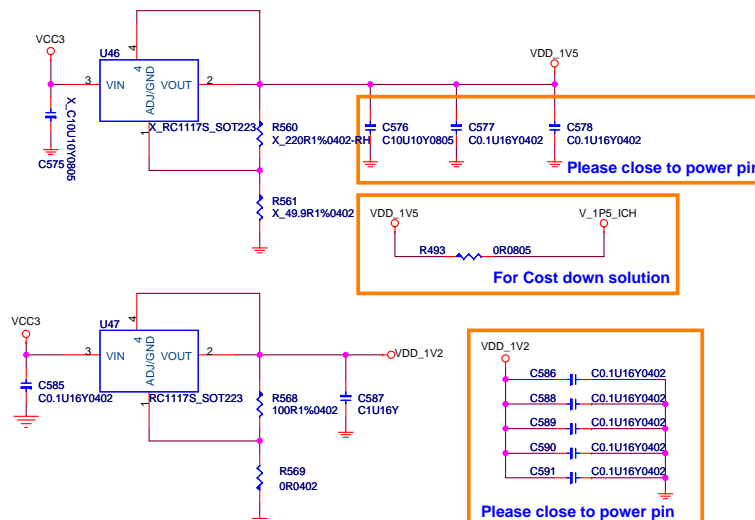
L02-8008074-J07 FOR BEAD



Analog power for internal voltage regulator, crystal oscillator, and PLL.



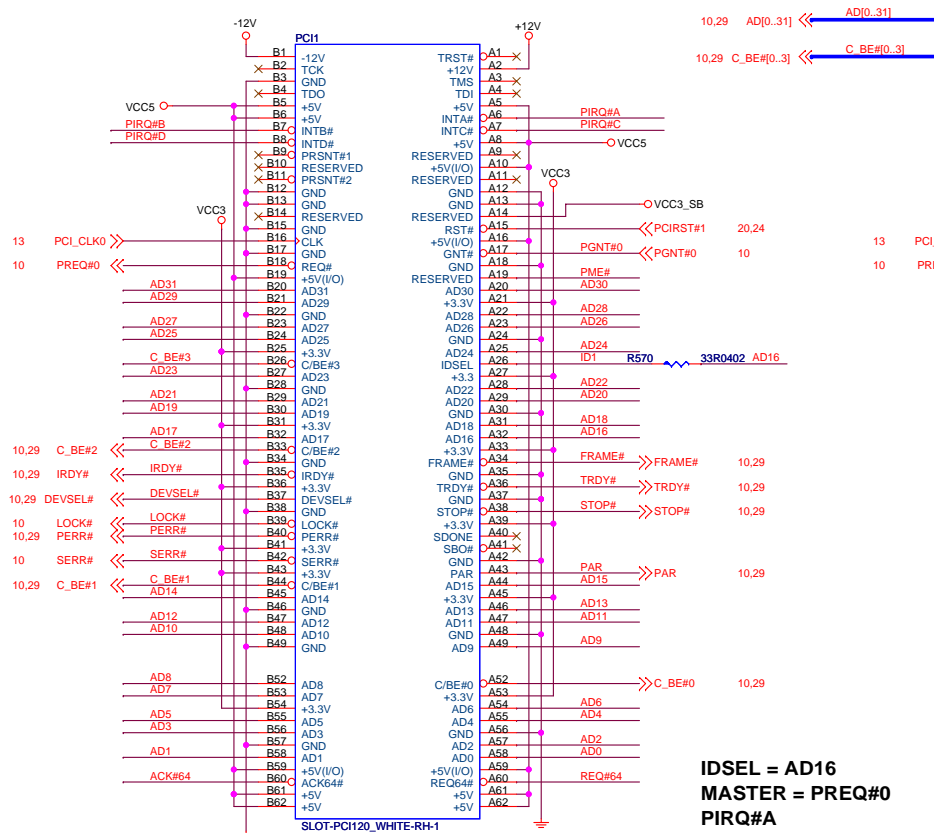
3.3V analog power for serial ATA PHY.



Chipset auto detect cable type.

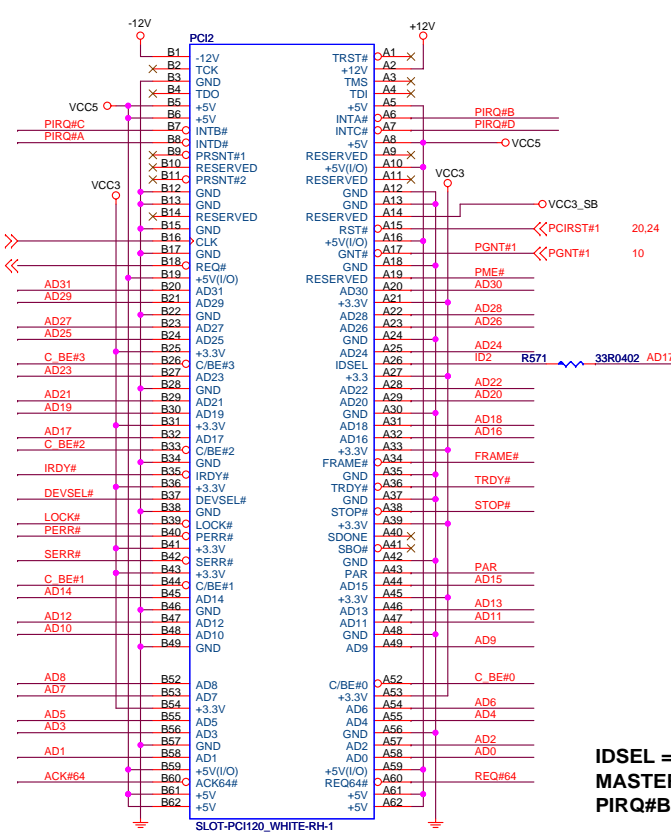
PCI 2.2 Slot 1 & 2

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



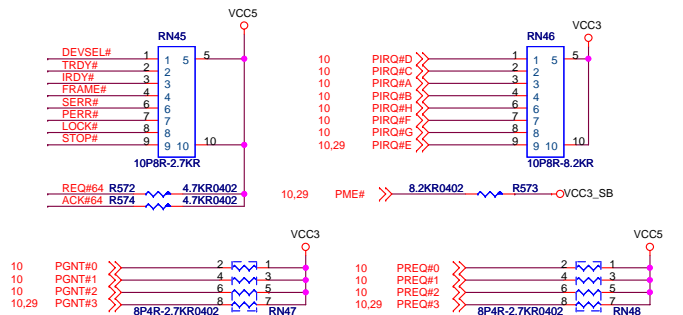
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI SLOT 2 (PCI VER: 2.2 COMPLY)

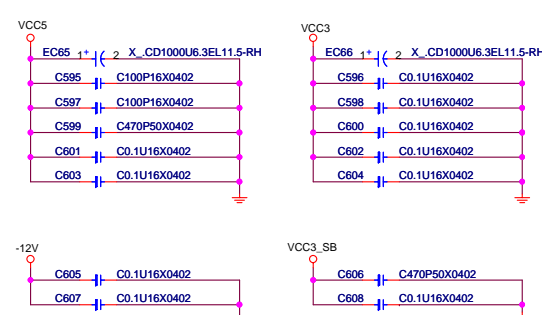


IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS




PCI SLOT DECOUPLING CAPACITORS



Please close to slot power pin

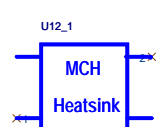
EMI Solution

 MICRO-START INTL CO.,LTD.		
Title EMI Solution		
Size	Document Number MS-7362	Rev 1.0
Date:	Tuesday, March 27, 2007	Sheet 32 of 40

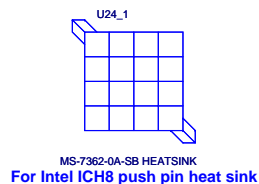
Manual Part

PCB1
MS-7362-1.0,RED OSP
P80-0736210-D05
P80-0736210-Y34

BAT1_1
BAT-BCR2032P-RH



For Intel P965 push pin heat sink



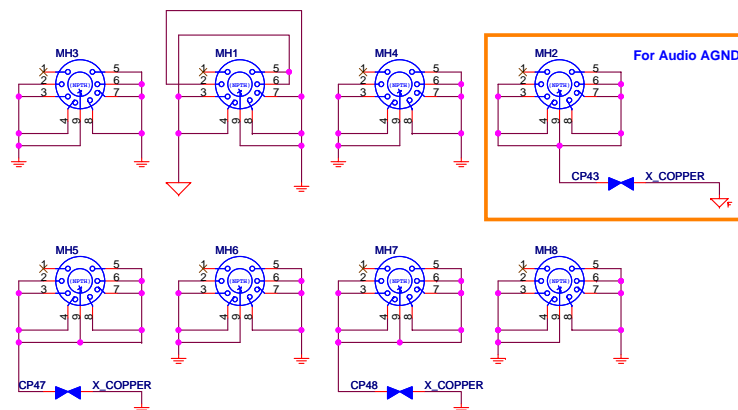
MS-7362-0A-SB HEATSINK
For Intel ICH8 push pin heat sink

U901
Intel NH82801HB
B0(SL9MN)
X_[INTEL-NH82801HB-B0-RH]
For Basic Function version,(Intel ICH8)

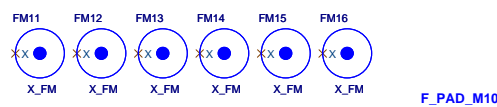
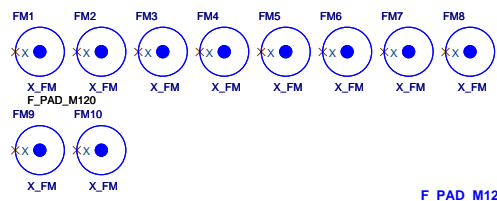
U902 X_100R0805
For VTT_SET circuit.

U903 X_F-SMD1812P260TF-RH
For Full Function version,(Front USB port fuse)

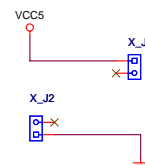
PCB Mounting Holes



Optics Orientation Holes



Simulation



ICH8DH GPIO Pin Definition

GPIO Pin	Type	Default	Function	Power	Multi-Function	Pin-out
GPIO 0	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	Yes	AF9
GPIO 1	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	Yes	AF5
GPIO 2	I/O	GPI	PIRQ#E pull-up to VCC3 with 10K	VCC3		D5
GPIO 3	I/O	GPI	PIRQ#F pull-up to VCC3 with 10K	VCC3		F10
GPIO 4	I/O	GPI	PIRQ#G pull-up to VCC3 with 10K	VCC3		G11
GPIO 5	I/O	GPI	PIRQ#H pull-up to VCC3 with 10K	VCC3		F9
GPIO 6	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	Yes	AE6
GPIO 7	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	Yes	AC8
GPIO 8	I/O	GPI	SIO_PME# connect to SIO,pull_up VCC3_SB with 10K	VCC3_SB	No	AE16
GPIO 9	I/O	MGPIO3	Pull-up to VCC3_SB with 10K directly	VCC3_SB	Yes	AG18
GPIO 10	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	Yes	AF20
GPIO 11	I/O	SMBALERT#	SMB_ALERT# pull-up to VCC3_SB with 10K	VCC3_SB		AF21
GPIO 12	I/O	GPI	Clear password pull-up to VBT with 1M	VBT	No	AC19
GPIO 13	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	No	AF18
GPIO 14	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	Yes	AH24
GPIO 15	I/O	GPO	NC	VCC3_SB	No	AE21
GPIO 16	I/O	GPO	SIO HWM_INT,pull_up VCC3 with 10K(change to GPI)		No	AE11
GPIO 17	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AC7
GPIO 18	I/O	GPO	NC		No	AC11
GPIO 19	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AD8
GPIO 20	I/O	GPO	NC		No	AG8
GPIO 21	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AB11
GPIO 22	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	Yes	AE7
GPIO 23	I/O	LDRQ1#	LDRQ_1# pull_up VCC3 with 10K	VCC3	Yes	C3
GPIO 24	I/O	GPO	NC		Yes	AG23
GPIO 25	I/O	GPO	NC	3.3V_SB	No	AH17
GPIO 26	I/O	GPO	S4 STATE			AH25
GPIO 27	I/O	GPO	NC	3.3V_SB		AD20
GPIO 28	I/O	GPO	NC			AD15
GPIO 29	I/O	OC5#	OC#3 connect to USB connector	3.3V_SB		AE15
GPIO 30	I/O	OC6#	OC#4 connect to USB connector	3.3V_SB		AG13
GPIO 31	I/O	OC7#	OC#4 connect to USB connector	3.3V_SB		AF14
GPIO 32	I/O	GPO	SIO_SMI# connect to SIO,pull up VCC3 with 10k	VCC3	No	AH7
GPIO 33	I/O	GPO	NC		No	AG7
GPIO 34	I/O	GPO	NC		No	AG12
GPIO 35	I/O	GPO	NC			AD12
GPIO 36	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AF8
GPIO 37	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AD9
GPIO 38	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AH6
GPIO 39	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AC10
GPIO 40	I/O	OC1#	OC#1 connect to USB connector	VCC3		AH14
GPIO 41	I/O	OC2#	OC#2 connect to USB connector	VCC3		AG14
GPIO 42	I/O	OC3#	OC#2 connect to USB connector	VCC3		AG15
GPIO 43	I/O	OC4#	OC#3 connect to USB connector	VCC3		AH15
GPIO 44	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AF7
GPIO 45	I/O	CPUPWRGD	H_PWRGD connect to CPU	VTT_OUT		AF25
GPIO 46	I/O	REQ1#	REQ1 pull-up to VCC5 with 10K	VCC5	Yes	C16
GPIO 47	I/O	GNT1#	GNT1#		Yes	A15
GPIO 48	I/O	REQ2#	REQ2 pull-up to VCC5 with 10K	VCC5	Yes	B16
GPIO 49	I/O	GNT2#	GNT2#		Yes	D17
GPIO 50	I/O	REQ3#	REQ3 pull-up to VCC5 with 10K	VCC5	Yes	A9
GPIO 51	I/O	GNT3#	GNT3#		Yes	B9

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK	PCI Reset
VIA VT6308P	PIRQ#E	PREQ#3 PGNT#3	AD23	1394_PCLK	PCIRST#2
PCI slot 1	PIRQ#A	PREQ#0 PGNT#0	AD16	PCI_CLK0	PCIRST#1
PCI slot 2	PIRQ#B	PREQ#1 PGNT#1	AD17	PCI_CLK1	PCIRST#1

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	0A0H	P_DDR0_A / N_DDR0_A P_DDR1_A / N_DDR1_A P_DDR2_A / N_DDR2_A
DIMM 2	0A2H	P_DDR3_A / N_DDR3_A P_DDR4_A / N_DDR4_A P_DDR5_A / N_DDR5_A
DIMM 3	0A4H	P_DDR0_B / N_DDR0_B P_DDR1_B / N_DDR1_B P_DDR2_B / N_DDR2_B
DIMM 4	0A6H	P_DDR3_B / N_DDR3_B P_DDR4_B / N_DDR4_B P_DDR5_B / N_DDR5_B

SMBus Distribution

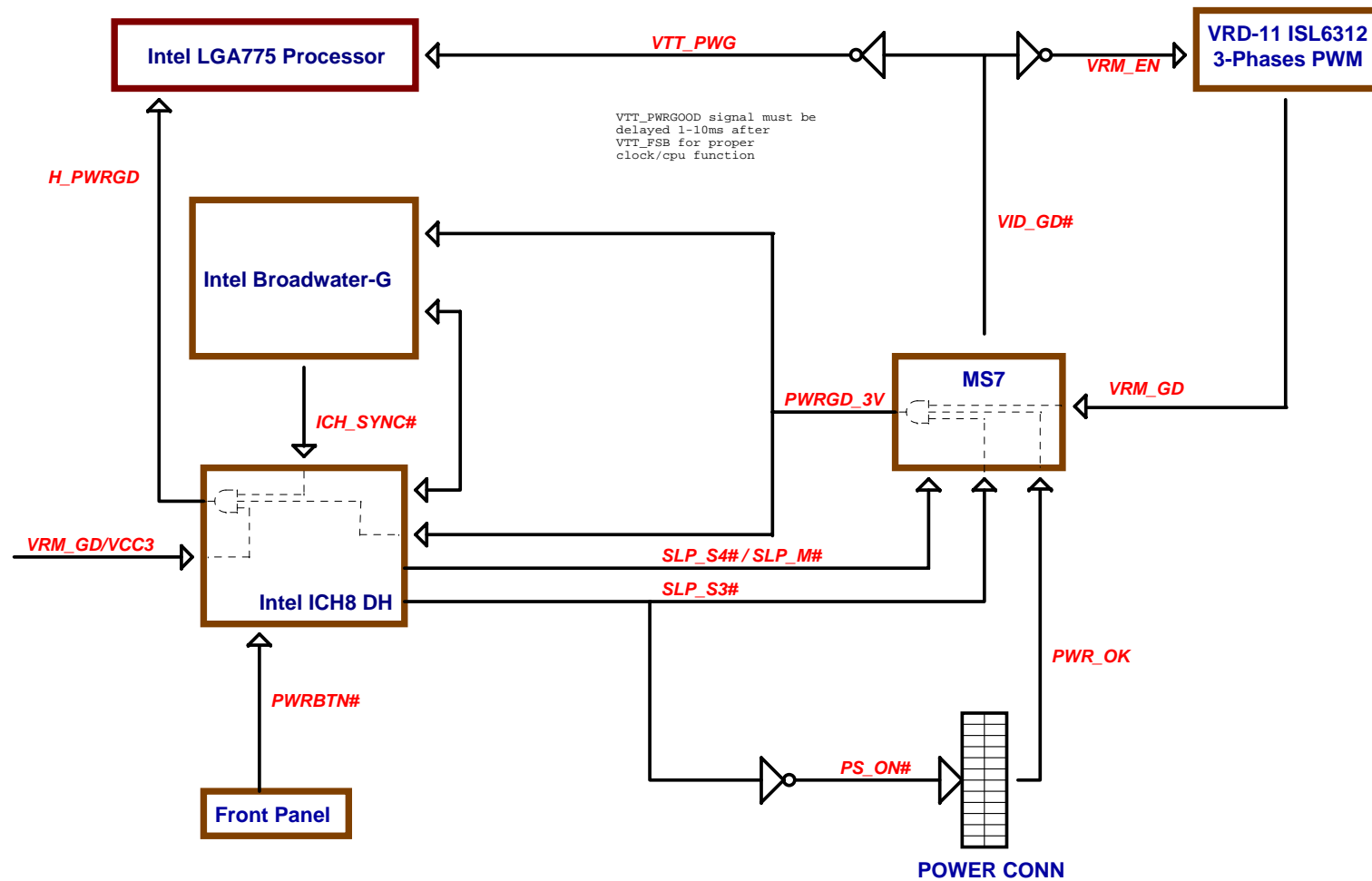
SMBus	Power	Load
SMBDATA_MAIN SMBCLK_MAIN	VCC3_SB	ICH8 , Clock Gen , Super I/O , DDR II , PCI Express x16 , PCI Express x1 , MS7 , PWM

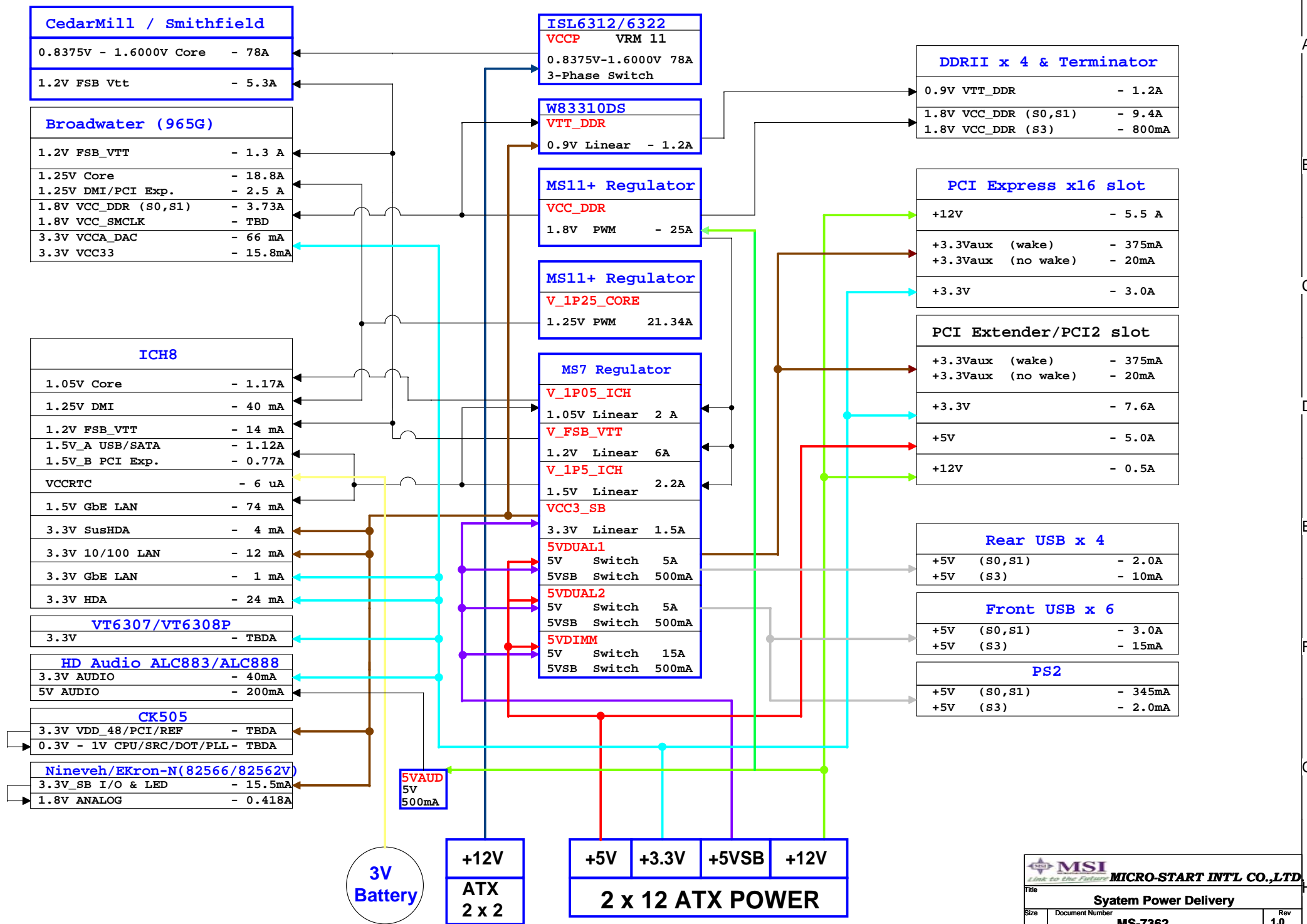
Jumper Setting

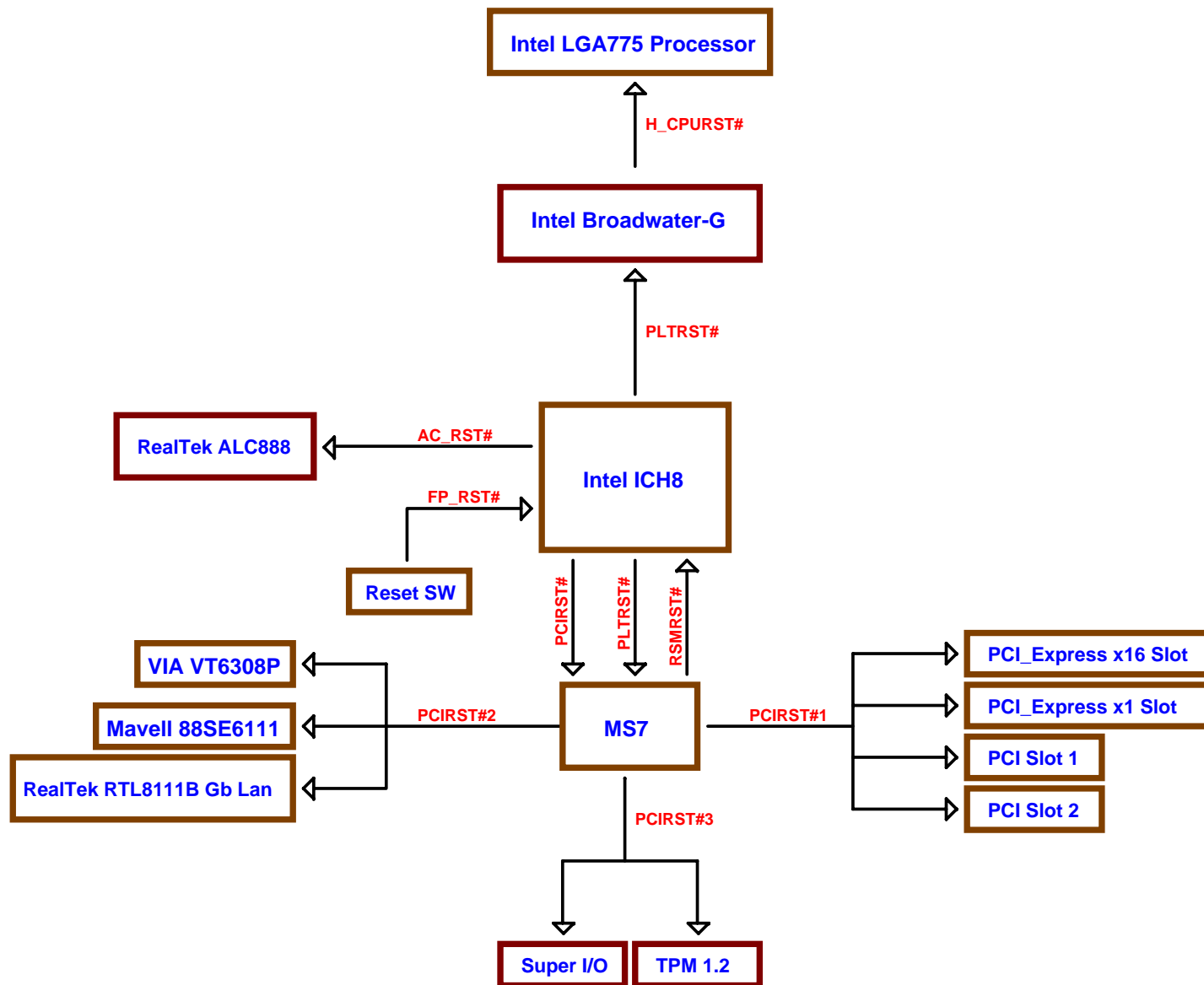
JBAT1	(1-2) Normal	(2-3) Clear
-------	--------------	-------------

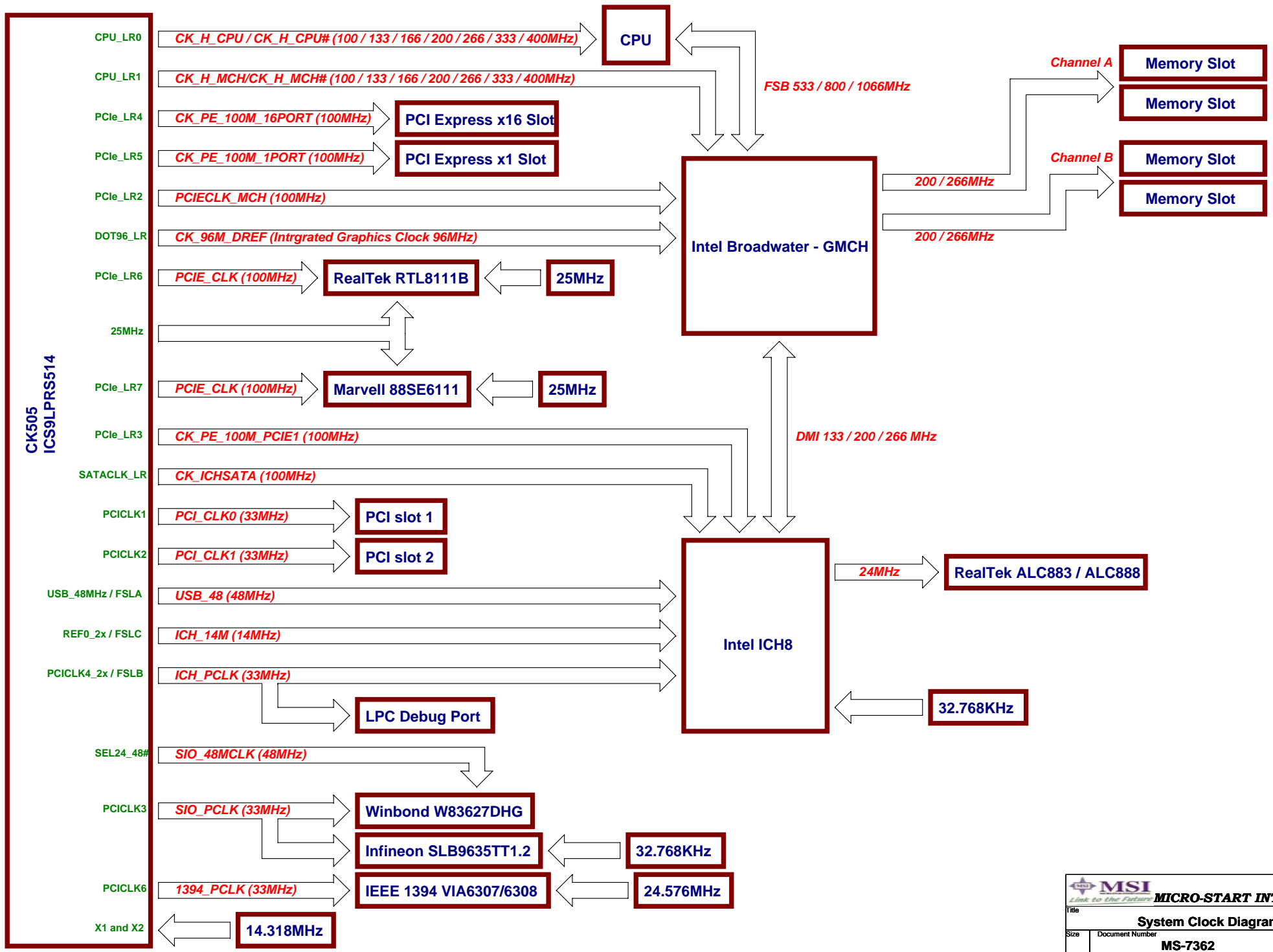
PCI Reset Device

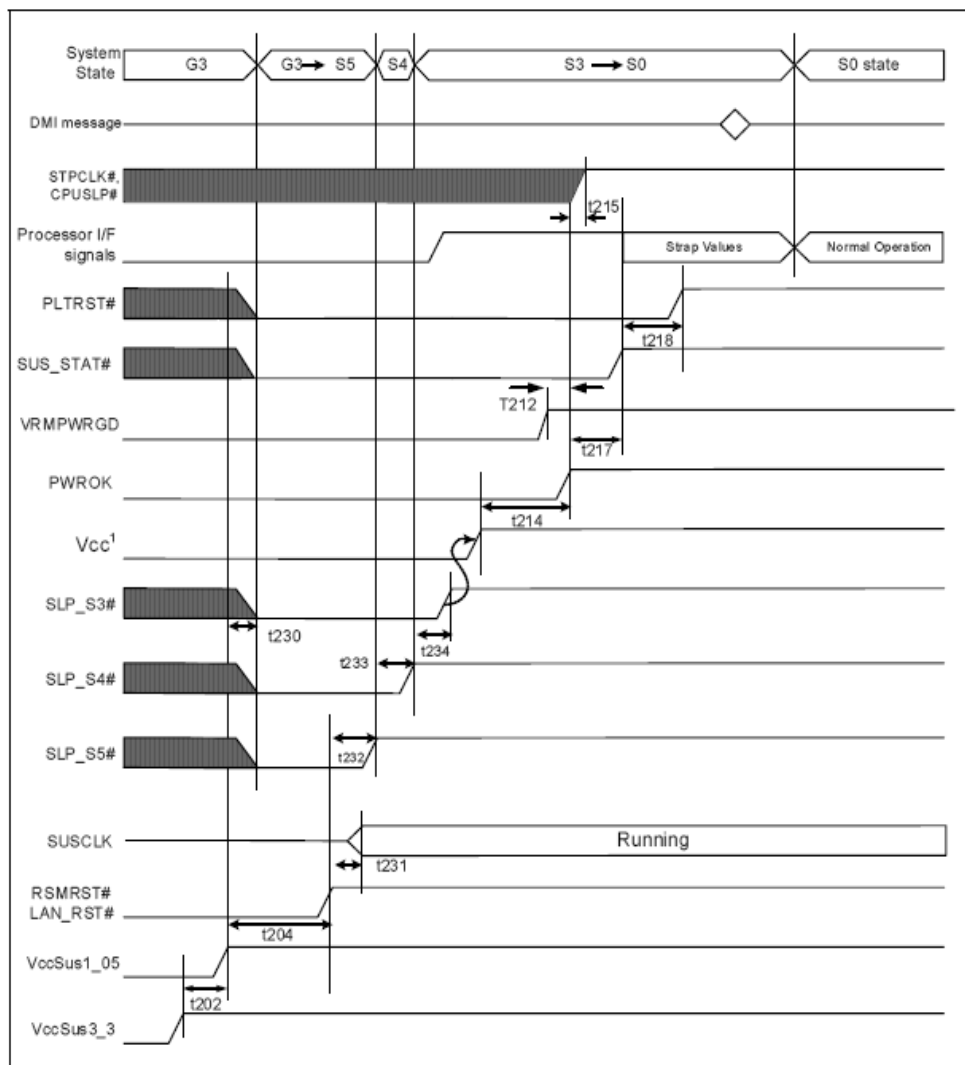
Signal	Device
PLTRST#	MS7 , NB
PCIRST_ICH8#	MS7
PCIRST#1	PCI1 , PCI2 , PCIE x16 , PCIE x1
PCIRST#2	VT6308P , 88SE6111
PCIRST#3	TPM , Super I/O












NOTES:

1. Vcc includes Vcc1_5_A, Vcc1_5_B, Vcc3_3, Vcc1_05, VccUSBPLL, VccDMIPLL, VccSATAPLL, and V5REF.

- 2006-12-29
1. Create new schematic for 7362-0A
- 2007-01-02
1. New schematic net-in
- 2007-01-03
1. Placement and Layout



MICRO-START INTL CO.,LTD.

Title

Project History

Size

Document Number

Rev

MS-7362

1.0

Date: Tuesday, March 27, 2007

Sheet 40 of 40